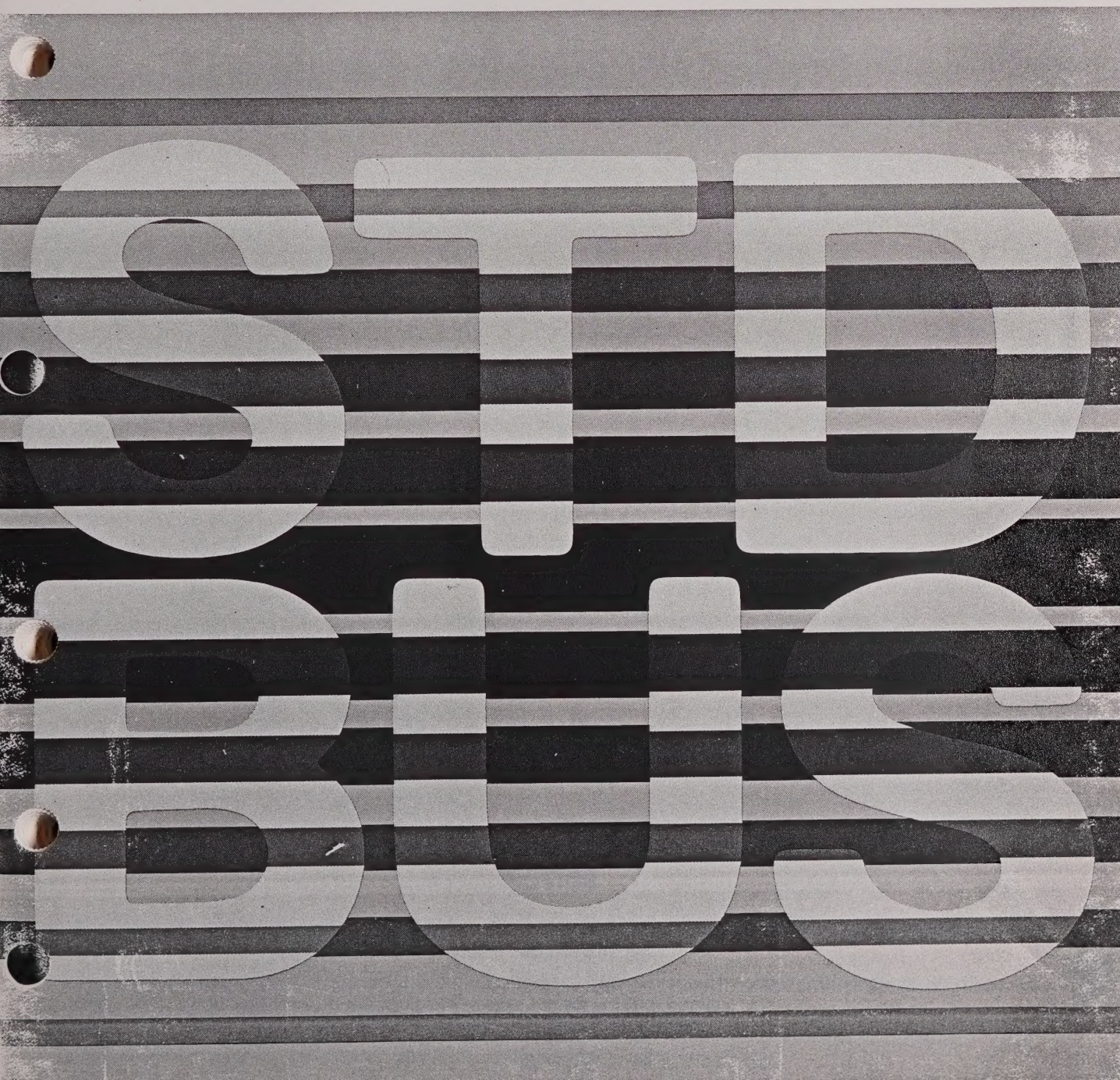
PRO-LOG® CORPORATION

STD 7000

7507 General Purpose Interface Card

USER'S MANUAL



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STD 7000

7507

General Purpose Interface Card

USER'S MANUAL

FOREWORD

This manual explains how to use the Pro-Log 7507 General Purpose Interface card. It is structured to reflect the answers to basic questions you might ask yourself about the 7507. We welcome your suggestions on how we can improve our instructions.

The 7507 is part of the Pro-Log Series 7000 STD BUS hardware. Our products are modular, and designed and built with second-sourced parts that are industry standards. They provide industrial managers with the means of using their own people to control the design, production, and maintenance of the products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, we teach courses on how to design with and use microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: the Microprocessor User's Guide and the STD BUS Specification and Practice. If you would like a copy of these documents, please write to us on your company letterhead.

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PURPOSE AND MAIN FEATURES

INTRODUCTION

The 7507 is a TTL I/O card that provides an interface between the STD BUS and the industry standard I/O module mounting rack (OPTO-22 Corp. or equivalent). This interface card controls up to 24 input or output modules for either AC or DC in any combination and position on the I/O module mounting rack. The I/O module mounting rack can be separated from the interface card by up to 10 feet (3.05m) of 50-conductor ribbon cable. Also, the interface card can drive one or more addressable I/O module mounting racks (Adatek Corp. or equivalent). Using these racks, one interface card can drive up to 512 I/O modules.

The 7507 can be used as a short-distance (3.05m) parallel data communications card. The three 8-bit read/write ports transmit and receive data and provide handshake signals. This capability is useful for data transfers between PROM programmers (such as Pro-Log's M980), printers, and other STD BUS systems.

The 7507 is also useful as a general purpose TTL interface card. Three 8-bit read/write ports control 24 bidirectional signal lines. In addition, an output port-controlled power source rated for +4.75V at 500 mA is provided. An LED assembly, visible from the card edge, monitors the state of the power source and three signal lines.

Connection to the 7507 is supplied through a 50-pin card edge connector. Adjacent grounds are provided for each signal line for use in ribbon cable or discrete wire cable assemblies.

MAIN FEATURES

- Up to 24 directly addressable I/O modules per 7507
- Module control in any position or combination
- Allows use of industry standard industrial I/O module mounting racks
- Low pass input filters for noisy industrial environments
- Single +5V operation
- Two-year warranty

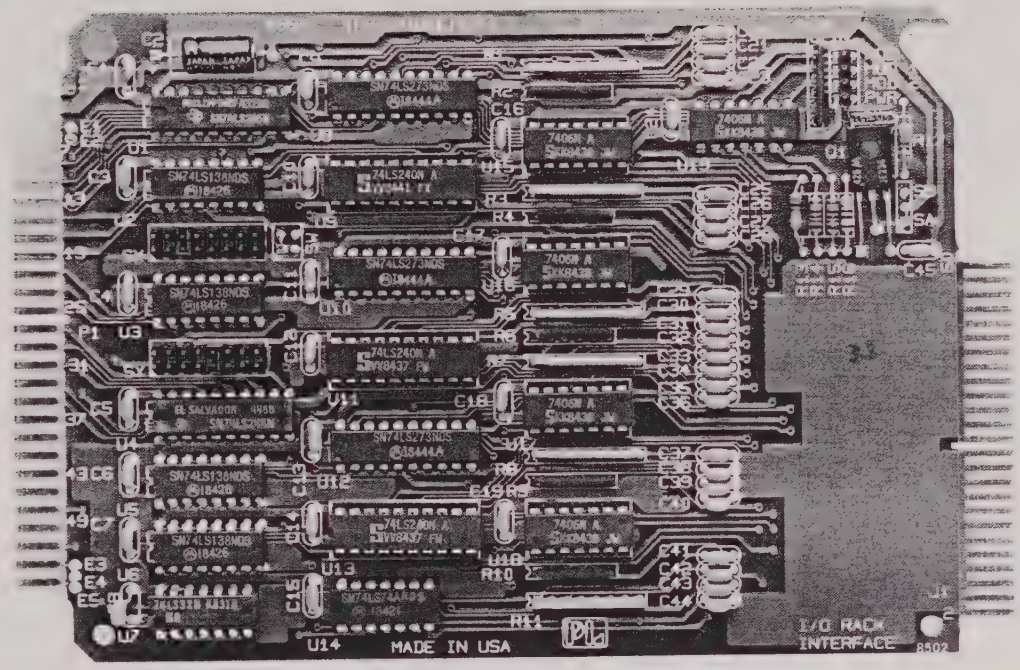


Figure 1-1. 7507 I/O Rack Interface Card

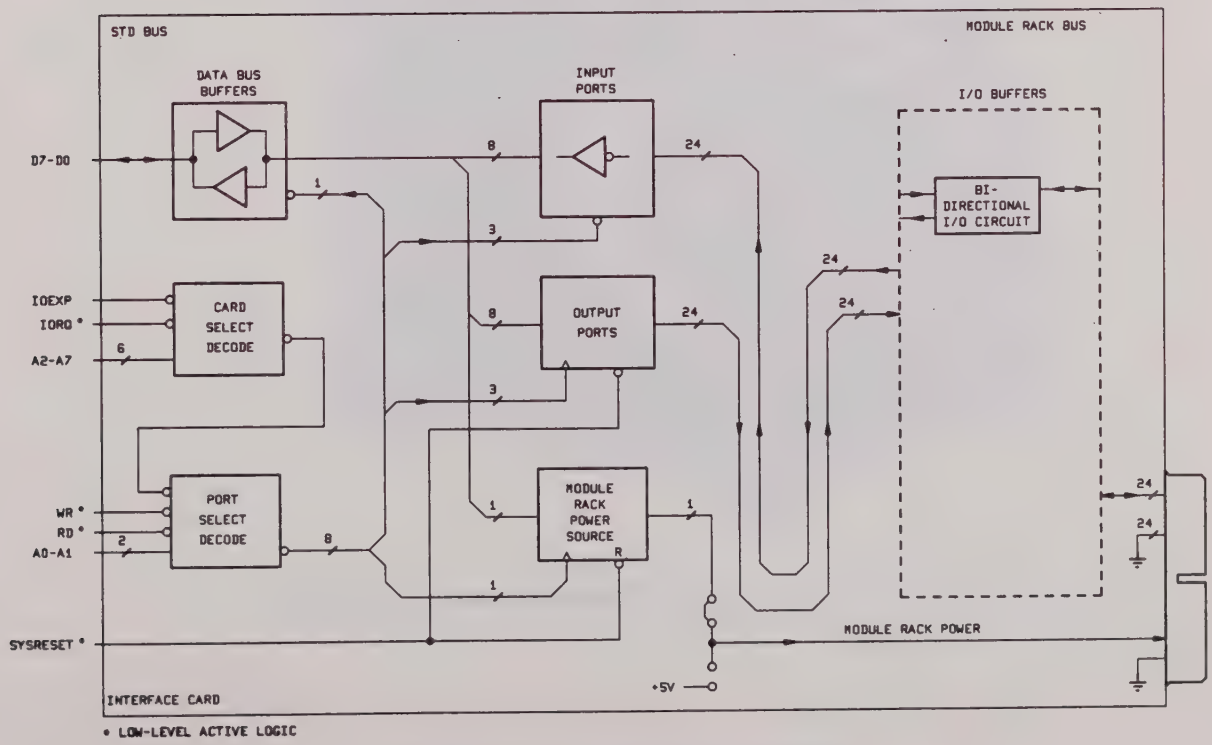
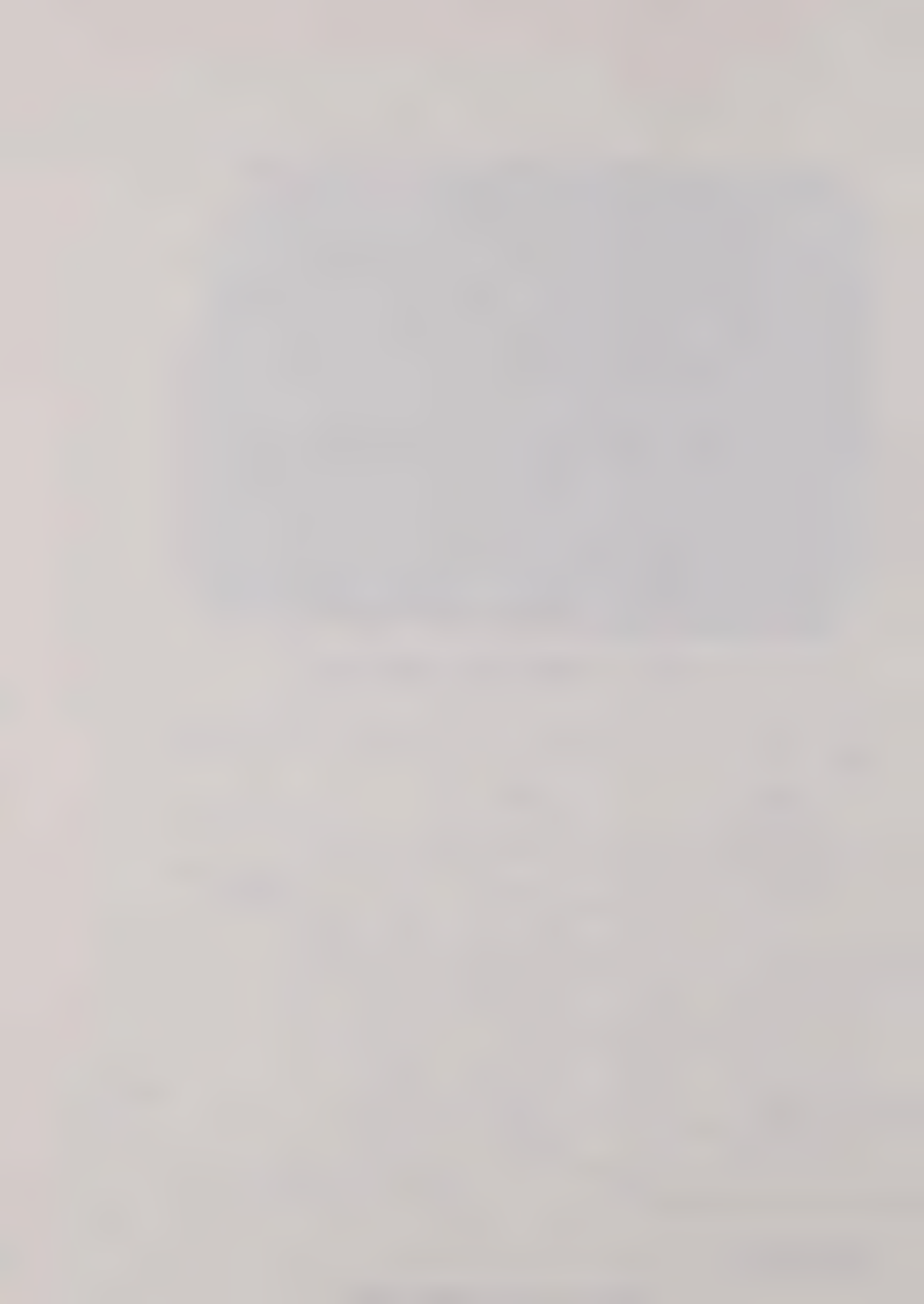


Figure 1-3. Block Diagram (7507)



INTRODUCTION

This section explains the functions and options of the card to consider before using the card in your system. This section also covers the product specifications.

INSTALLATION

> **CAUTION**
>
> To prevent possible damage to the STD BUS system, ensure that power is **off** before inserting or removing the card into/from the rack.

The interface card operates as part of an STD BUS card rack system. It plugs directly into the STD BUS backplane. The interface card can be inserted into any slot in the card. It should be inserted with the card ejector tab at the top of the card, as shown in figure 2-1.

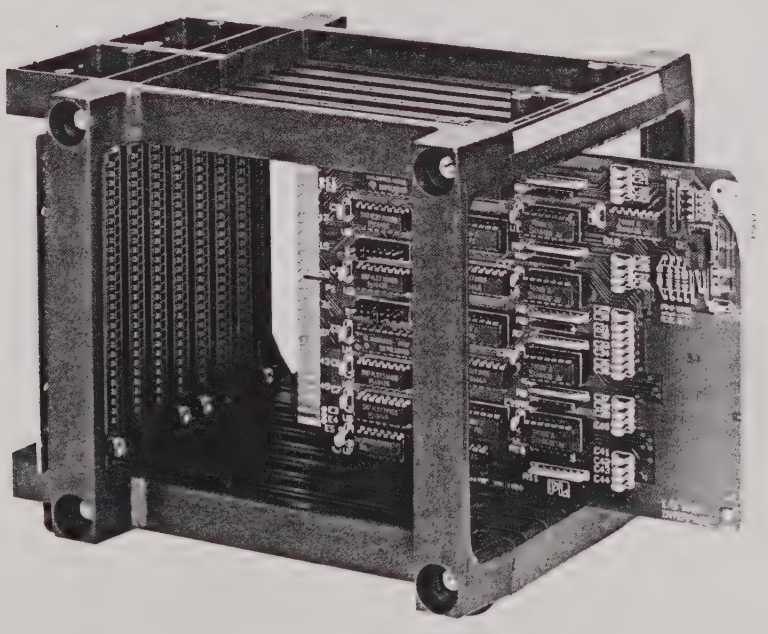


Figure 2-1. Installation of Interface Card in an STD BUS Rack

I/O MAPPED CARD ADDRESSING

The 7507 occupies four consecutive I/O addresses. As shipped, the card is mapped at port addresses 50H to 53H. These addresses can be retained or changed. The card's port addresses must differ from all other I/O port addresses in the system. If they do not differ, multiple cards respond to the same READ instruction, resulting in bus contention.

The interface card can be remapped anywhere within the 256-port addressing range. To change the I/O addressing of the interface cards, jumpers SX and SY must be changed. Figure 2-2 shows the jumper locations and figure 2-3 shows the jumper positions required for alternate mappings.

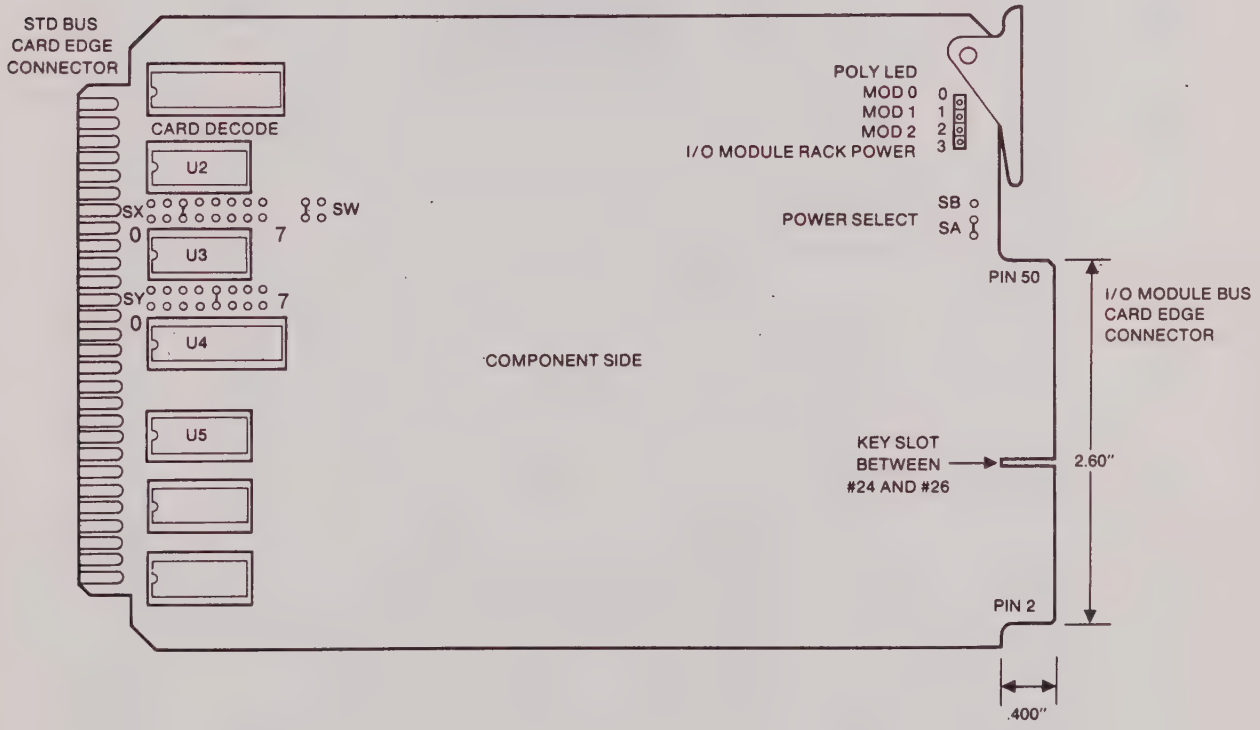


Figure 2-2. Physical Location of Components (7507)

PORTS	JUMPER WIRES
00	SX0, SY0
01	
02	
03	
04	SX0, SY1
05	
06	
07	
08	SX0, SY2
09	
0A	
0B	
0C	SX0, SY3
0D	
0E	
0F	
10	SX0, SY4
11	
12	
13	
14	SX0, SY5
15	
16	
17	
18	SX0, SY6
19	
1A	
1B	
1C	SX0, SY7
1D	
1E	
1F	
20	SX1, SY0
21	
22	
23	
24	SX1, SY1
25	
26	
27	
28	SX1, SY2
29	
2A	
2B	
2C	SX1, SY3
2D	
2E	
2F	
30	SX1, SY4
31	
32	
33	
34	SX1, SY5
35	
36	
37	
38	SX1, SY6
39	
3A	
3B	
3C	SX1, SY7
3D	
3E	
3F	

PORTS	JUMPER WIRES
40	SX2, SY0
41	
42	
43	
44	SX2, SY1
45	
46	
47	
48	SX2, SY2
49	
4A	
4B	
4C	SX2, SY3
4D	
4E	
4F	
50	SX2, SY4
51	
52	
53	
54	SX2, SY5
55	
56	
57	
58	SX2, SY6
59	
5A	
5B	
5C	SX2, SY7
5D	
5E	
5F	
60	SX3, SY0
61	
62	
63	
64	SX3, SY1
65	
66	
67	
68	SX3, SY2
69	
6A	
6B	
6C	SX3, SY3
6D	
6E	
6F	
70	SX3, SY4
71	
72	
73	
74	SX3, SY5
75	
76	
77	
78	SX3, SY6
79	
7A	
7B	
7C	SX3, SY7
7D	
7E	
7F	

PORTS	JUMPER WIRES
80	SX4, SY0
81	
82	
83	
84	SX4, SY1
85	
86	
87	
88	SX4, SY2
89	
8A	
8B	
8C	SX4, SY3
8D	
8E	
8F	
90	SX4, SY4
91	
92	
93	
94	SX4, SY5
95	
96	
97	
98	SX4, SY6
99	
9A	
9B	
9C	SX4, SY7
9D	
9E	
9F	
A0	SX5, SY0
A1	
A2	
A3	
A4	SX5, SY1
A5	
A6	
A7	
A8	SX5, SY2
A9	
AA	
AB	
AC	SX5, SY3
AD	
AE	
AF	
B0	SX5, SY4
B1	
B2	
B3	
B4	SX5, SY5
B5	
B6	
B7	
B8	SX5, SY6
B9	
BA	
BB	
BC	SX5, SY7
BD	
BE	
BF	

PORTS	JUMPER WIRES
C0	SX6, SY0
C1	
C2	
C3	
C4	SX6, SY1
C5	
C6	
C7	
C8	SX6, SY2
C9	
CA	
CB	
CC	SX6, SY3
CD	
CE	
DF	
D0	SX6, SY4
D1	
D2	
D3	
D4	SX6, SY5
D5	
D6	
D7	
D8	SX6, SY6
D9	
DA	
DB	
DC	SX6, SY7
DD	
DE	
DF	
E0	SX7, SY0
E1	
E2	
E3	
E4	SX7, SY1
E5	
E6	
E7	
E8	SX7, SY2
E9	
EA	
EB	
EC	SX7, SY3
ED	
EE	
EF	
F0	SX7, SY4
F1	
F2	
F3	
F4	SX7, SY5
F5	
F6	
F7	
F8	SX7, SY6
F9	
FA	
FB	
FC	SX7, SY7
FD	
FE	
FF	

Figure 2-3. Port Address Mapping (7507)

WIRE JUMPERS

Various optional functions are selected by wire jumpers. When removing and replacing these jumpers, cut the jumper in half, then desolder and remove each half individually. Any remaining solder should be removed before new jumpers are installed. This procedure prevents damage to circuit traces.

Wire jumpers can be replaced by permanent 0.025-inch square post headers which can be connected by slip-on/slip-off connectors. Part numbers for these connectors and headers are listed in figure 2-4. Figure 2-2, page 2-2, shows the locations of these jumpers.

PART	MANUFACTURER PART NUMBER	
	ELCO CORP	BERG ELECTRONICS
2-Pin Header	00 8261 02 32 00 852	65611-102
4-Pin Header	00 8261 04 32 00 852	65611-104
6-Pin Header	00 8261 06 32 00 852	65611-106
8-Pin Header	00 8261 08 32 00 852	65611-108
Connector	00 8261 02 42 00 870	—

Figure 2-4. Part Numbers for Option Jumpers (7507)

IOEXP

The interface card can be configured to operate with either a high or low active IOEXP. The card is shipped from Pro-Log configured for a low active IOEXP. If a high active IOEXP is desired, jumper SW must be changed. Figure 2-5 shows how to configure these jumpers.

IOEXP ENABLE STATE	JUMPER SW0	JUMPER SW1
Low*	connected	OPEN
High	OPEN	connected

*As shipped.

Figure 2-5. IOEXP Jumpers (7507)

MODULE RACK POWER

The I/O module mounting racks to which the 7507 interfaces require +5V to be supplied. The interface card provides the required voltage (4.75V at 500 mA) via the interface connector.

The interface card has on-card jumpers that configure the power output pin in one of three ways. As shipped, the module power output pin is under software control. Bit 7 of port 53H turns power off or on.

A second way to configure the module power line is to output power directly from the Vcc of the STD BUS system to the I/O module mounting rack. To bypass the port-controlled +4.75V power source, move the wire jumper from location SA to location SB. With this feature the I/O module rack has power any time that the STD BUS system VCC is on.

The third way to configure the module-power line is to disconnect it altogether by disconnecting both jumpers SA and SB. In this configuration, the I/O module mounting rack can be powered by an external power source. Figure 2-6 shows the power jumper options in table form.

MODULE-POWER OPTION	JUMPER SA	JUMPER SB
Software controlled*	connected	OPEN
Always ON	OPEN	connected
Always OFF	OPEN	OPEN

*As shipped.

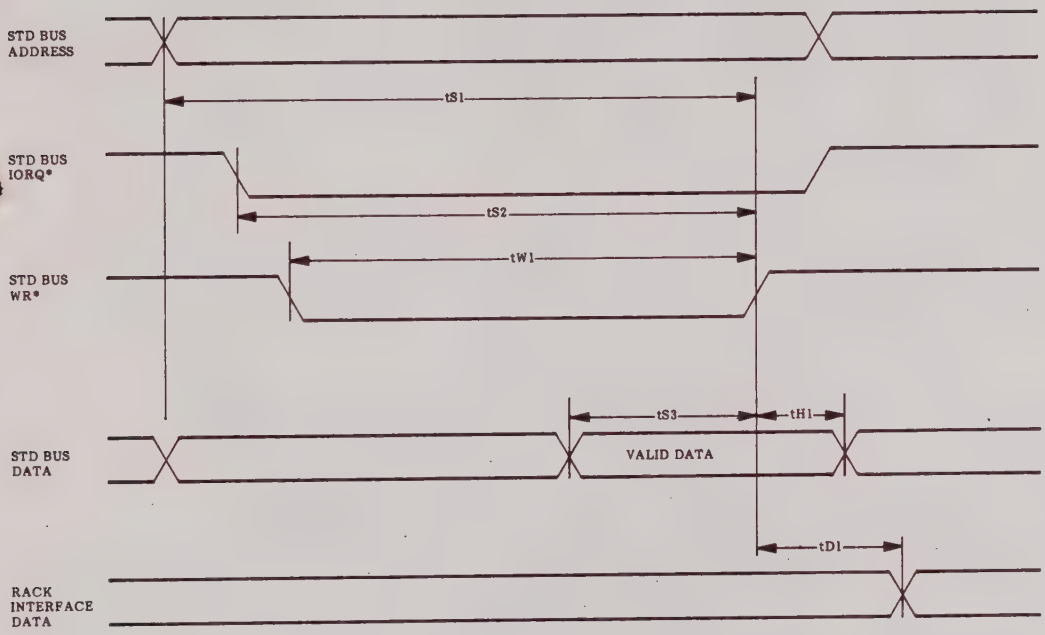
Figure 2-6. Power Jumper Options (7507)

POWER INDICATOR LED

The state of the I/O module mounting rack current is indicated by D1-4 LED on the interface card (on Vcc = 4.75V, off Vcc = +0V). See Physical Location of Components, figure 2-2, page 2-2.

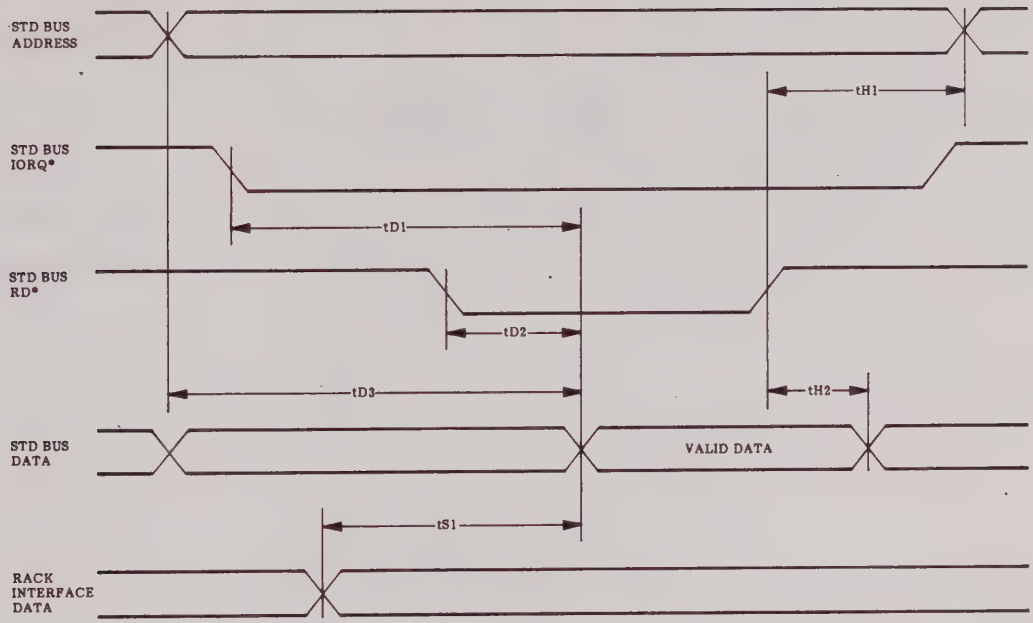
TIMING SPECIFICATIONS

Figures 2-7 and 2-8 show the timing of the I/O rack interface card.



SYMBOL	PARAMETER	MIN	MAX	UNITS
tD1	Data delay from IORQ* active		135	ns
tD2	Data delay from RD* active		110	ns
tD3	Data delay from address valid		200	ns
tH1	Address hold after RD* inactive	10		ns
tH2	Data hold after RD* inactive	15		ns
tS1	Rack interface data setup before STD data valid		27	µs

Figure 2-7. Read Timing (7507)



SYMBOL	PARAMETER	MIN	MAX	UNITS
tD1	Rack interface data delay from WR* inactive		105	ns
tH1	Data hold after WR* inactive	55		ns
tS1	Address setup before WR* inactive	190		ns
tS2	IORQ* setup before WR* inactive	125		ns
tS3	Data setup before WR* inactive	25		ns
tW1	WR* pulse width	85		ns

Figure 2-8. Write Timing (7507)

		RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
MNEM.	PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
VCC	Supply Voltage	4.75	5.00	5.25	0	7.00	Volts
TA	Free Air Temperature	0	25	65	-40	75	°C
ICC	Supply Current*	—	750	1000	—	—	mA

*Includes 500 mA load to external I/O module mounting rack.

Figure 2-9. I/O Rack Interface Card Electrical Specifications (7507)

MNEM.	PARAMETER	MIN	TYP	MAX	UNIT
V_{OL}	Low level interface voltage (at 10 mA current level)	—	—	.80	Volt
I_{OL}	Low level interface current (at 0.70V level)	—	—	20	mA
V_{OH}	High level interface voltage	4.75	—	5.25	Volt
I_{OH}	High level interface current (at 2.0V)	-3.0	—	—	mA
V_{EXT}	Supply voltage output to module rack	4.45	4.70	4.95	Volt
I_{EXT}	Supply current output to module rack	—	—	500	mA

Figure 2-10. User Interface Electrical Characteristics (7507)

MNEM.	PARAMETER	FROM	TO	MIN	TYP	MAX	UNIT
T_{PLH}	Propagation Time	STD DATA BUS	USER IFC	—	—	60	ns
T_{PHL}	Propagation Time	STD DATA BUS	USER IFC	—	—	65	ns
T_{PLH}	Propagation Time	USER IFC	STD DATA BUS	3	5	8	µs
T_{PHL}	Propagation Time	USER IFC	STD DATA BUS	11	18	27	µs

Figure 2-11. Switching Characteristics (7507)

	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
Free Air Temperature	0	25	65	-40	75	°C
Noncondensing Relative Humidity	5	—	95	5	95	%RH

Figure 2-12. Environmental Specifications (7507)

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
2	VCC		+5V	1		VCC	+5V
4	GND		GROUND	3		GND	GROUND
6			-5V	5			-5V
8	1	55	D7	7	55	1	D3
10	1	55	D6	9	55	1	D2
12	1	55	D5	11	55	1	D1
14	1	55	D4	13	55	1	D0
16			A15	15		1	A7
18			A14	17		1	A6
20			A13	19		1	A5
22			A12	21		1	A4
24			A11	23		1	A3
26			A10	25		1	A2
28			A9	27		1	A1
30			A8	29		1	A0
32		1	RD*	31		1	WR*
34			MEMRQ*	33		1	IORQ*
36			MEMEX	35		1	IOEXP
38			MCSYNC*	37			REFRESH*
40			STATUS 0*	39			STATUS 1*
42			BUSRQ*	41			BUSAK*
44			INTRQ*	43			INTAK*
46			NMIRQ*	45			WAITRQ*
48			PBRESET*	47		1	SYSRESET*
50			CNTRL*	49			CLOCK*
52	IN		PCI	51	OUT		PCO
54			AUX GND	53			AUX GND
56			AUX -V	55			AUX +V

* Low-level active logic

Figure 2-13. 7507 Edge Connector Pin List

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)				OUTPUT (LSTTL DRIVE)			
INPUT (LSTTL LOADS)				INPUT (LSTTL LOADS)			
MNEMONIC							MNEMONIC
GROUND			2	1	50	13	MOD 23*
			4	3	50	13	MOD 22*
			6	5	50	13	MOD 21*
			8	7	50	13	MOD 20*
			10	9	50	13	MOD 19*
			12	11	50	13	MOD 18*
			14	13	50	13	MOD 17*
			16	15	50	13	MOD 16*
			18	17	50	13	MOD 15*
			20	19	50	13	MOD 14*
			22	21	50	13	MOD 13*
			24	23	50	13	MOD 12*
			26	25	50	13	MOD 11*
			28	27	50	13	MOD 10*
			30	29	50	13	MOD 9*
			32	31	50	13	MOD 8*
			34	33	50	13	MOD 7*
			36	35	50	13	MOD 6*
			38	37	50	13	MOD 5*
			40	39	50	13	MOD 4*
			42	41	50	13	MOD 3*
			44	43	50	13	MOD 2*
			46	45	50	13	MOD 1*
			48	47	50	13	MOD 0*
GROUND			50	49	500mA		MODULE RACK PWR

* Low-level active logic

Figure 2-14. 7507 User Interface Pin List

MECHANICAL SPECIFICATIONS

The 7507 meets all general mechanical specifications of the STD BUS. The input connector clearance requirements vary according to the specific connector used. A 50-pin flat cable connector requires clearance of 0.250 inches on the component and circuit sides of the board.

PRO-LOG INTERCONNECT CABLE

The RC50-6 (figure 2-15) is a six-foot long 50-conductor ribbon cable with a 50-pin edge connector at each end. The keys provided with this cable should be used to ensure that the cable is never reversed during installation.

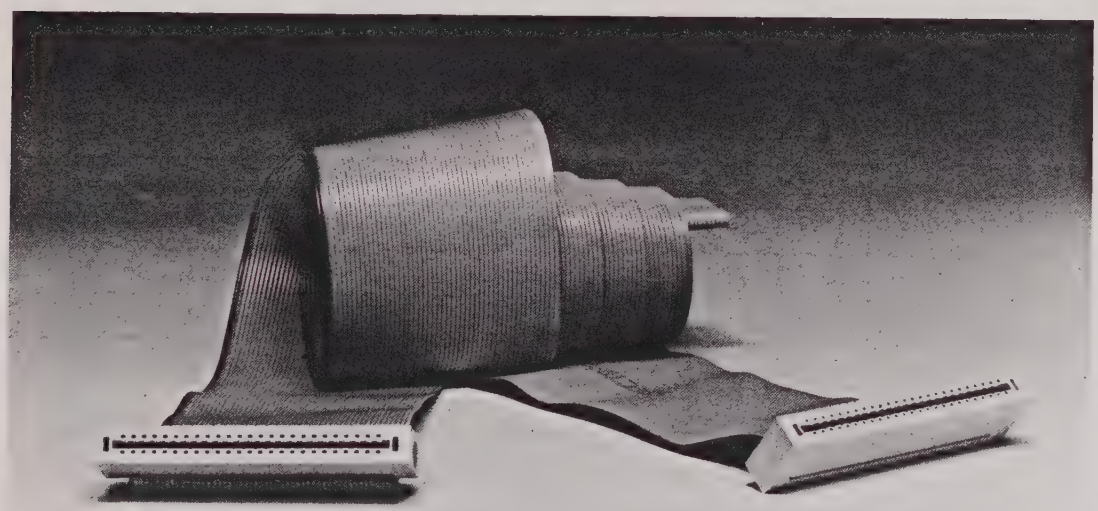


Figure 2-15. RC50-6 Compatible Cable (7507)

OTHER COMPATIBLE CONNECTORS

For discrete wire cable assemblies, a PC board edge connector with solder tail connections can be used in conjunction with a cable hood assembly to provide reliable, strain-relieved termination. The recommended 50-pin card edge connector is a Viking part number 3VH25/1JN5. This connector is used with a Viking Hood part number 036-0097-002 or equivalent (see figure 2-16).

MANUFACTURER	50-PIN CONNECTOR PART NUMBER	KEY P/N
Winchester	53-50-00	109-101037
Spectra Strip	807-5005-001	800-0711-001
Ansley	609-5015M	609-0005
3M	3415-001	3439.1000

NOTE: This list is for customer convenience. Many other manufacturers' connectors are compatible. For more information consult manufacturers' catalogs.

Figure 2-16. Compatible Connectors (7507)

INTRODUCTION

The 7507 is a general purpose TTL I/O card. It is designed for use with industry standard I/O module mounting racks (see figure 3-1). The I/O module mounting rack is a standalone board that accepts plug-in I/O modules. The modules come in four types — AC input, AC output, DC input, and DC output. The modules can be placed in any position on the mounting rack, allowing for any number and combination of module types. The modules are optically isolated and insensitive to harsh environments and electrical noise.

The I/O module mounting rack is a convenient way of translating from TTL signals to industrial voltages while keeping high voltages and discrete heavy gauge wires isolated from the STD BUS. The entire system is modular, making it easy to set up, modify, and maintain. Figure 3-2 lists some of the features and benefits of the system. Figure 3-3, page 3-3, shows a block diagram of a complete control system. Figure 3-4, page 3-3, gives sources for hardware, and figure 3-5, page 3-4, shows schematics of four types of modules.

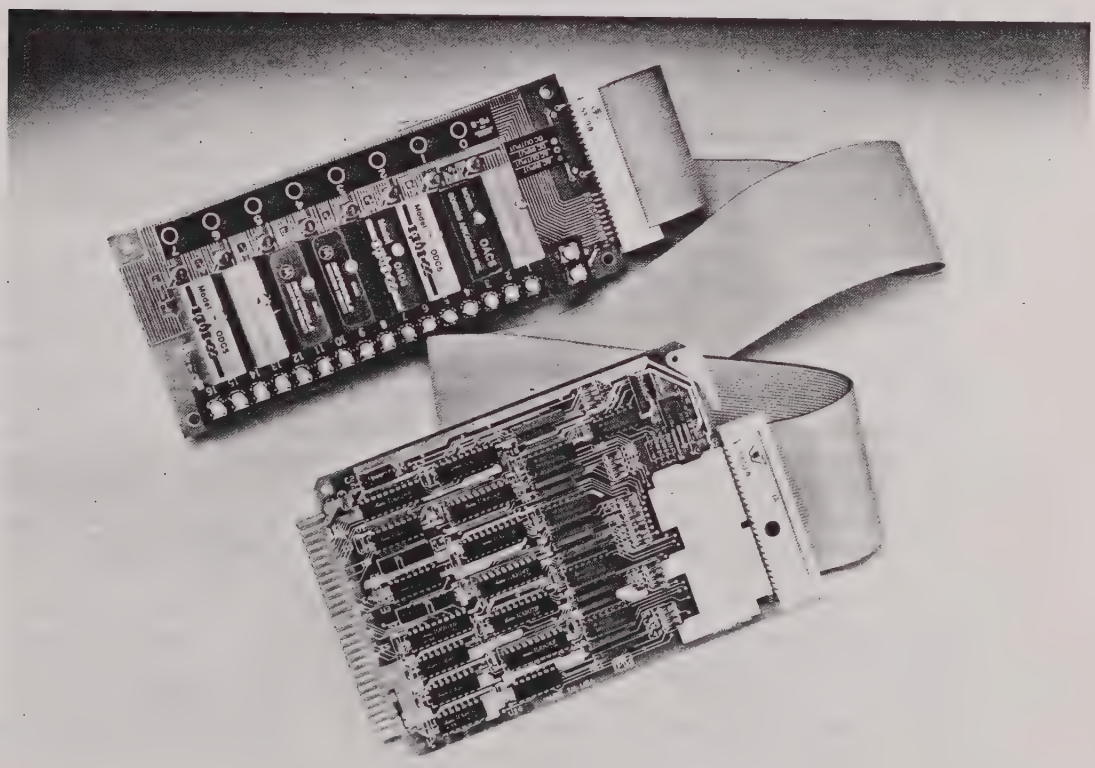


Figure 3-1. Industrial Interface System

FEATURES	BENEFITS
Industrial type barrier strip on mounting rack	Modules may be replaced without disturbing power wiring.
Plug-in modules	Meets Nema LCS 2-230. Power wiring need not be disconnected when changing modules.
Fully encapsulated modules	Provides immunity against adverse environments and increased thermal rating.
Individual plug-in fuses	Readily available fuses protect module and power wiring against short circuits.
LED status light for each module	Simplifies programming, setup, and troubleshooting.
2500 VAC isolation	Meets UL industrial specifications and VDE requirements.
8, 16, and 24 module racks available	Board size may be matched to system requirements.
Universal mounting racks	Allows use of any module in any position.
High voltage modules available	Allows operation on 240 VAC or up to 200 VDC.
High density package	24 modules fit in 19-inch rack.
UL Recognized	Safe, reliable.
Multisourced parts	Greater availability.
High industrial voltage and current away from STD BUS	Greater safety, reliability, and ease of maintenance.
No heavy gauge wires in STD BUS Card Rack	Ease of maintenance and installation.
Modules are opto-isolated	Immunity to fluctuations between digital ground and high-voltage ground.
Color-coded modules and module position markers	Reduces chances of using the wrong module or replacing with the wrong module.

Figure 3-2. Features and Benefits of the I/O Rack System

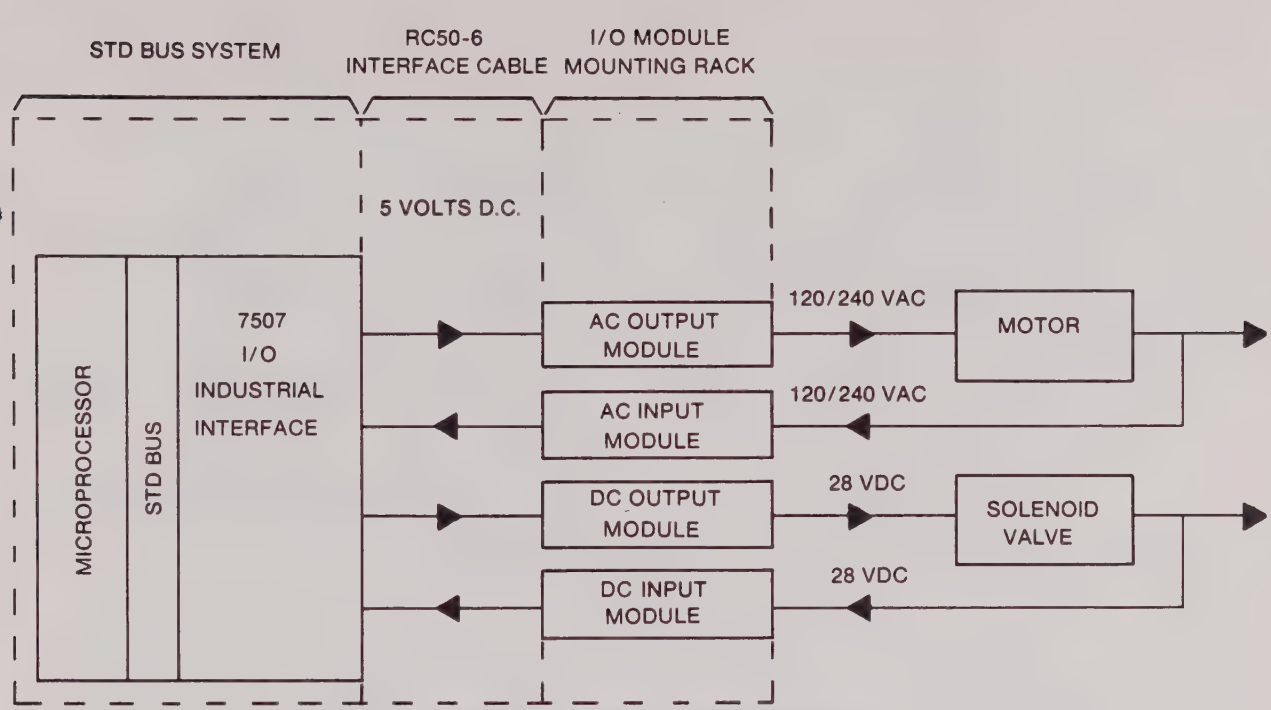


Figure 3-3. System Block Diagram

PART	MANUFACTURER
7507 RC50-6	Pro-Log Corporation
I/O Racks and Modules	Opto 22 Gordos Crydom Dutec
16 module[1] addressable rack	Opto 22
32 module[1] adressable rack	Adatek

[1] These are addressable racks which allow daisy chaining a number of racks on one cable. By this method, hundreds of modules can be controlled by one interface card.

NOTE: This partial list is provided for convenience only and is not intended to recommend any manufacturer.

Figure 3-4. Manufacturers of I/O Rack

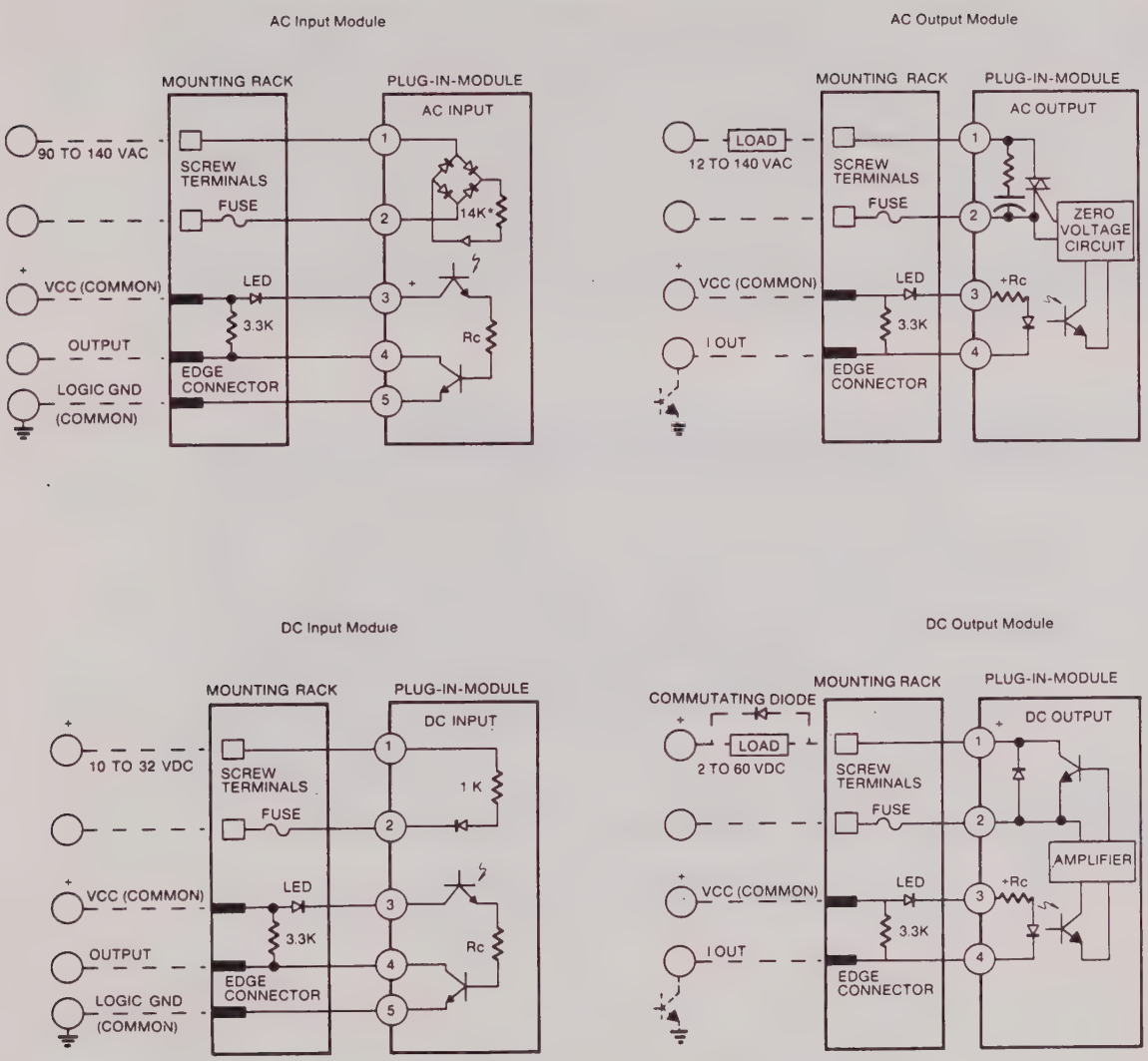


Figure 3-5. I/O Rack Module Schematics

I/O RACK INTERFACE

The interface card uses the industry standard I/O module bus to communicate with the I/O module mounting rack. The bus consists of 24 bidirectional data lines alternated with 24 ground lines, a switched +4.75V/500 mA power line, and a ground power line. These cables are routed over 50 conductor cable, up to ten feet (3.05m). The pinout of the interface connector (figure 2-14, page 2-11) directly matches the pinout of the I/O rack. The pinout and typical schematic of an I/O rack are given in figure 3-6. The interface card and the I/O racks use a 50-pin card edge connector with pins on 0.1-inch centers. Pro-Log provides an RC50-6 which meets these requirements (figures 3-1, page 3-1, and 2-15, page 2-12). Both the interface card and the I/O rack have keying slots on their card edge connectors. Keying the connectors prevents them from being attached incorrectly.

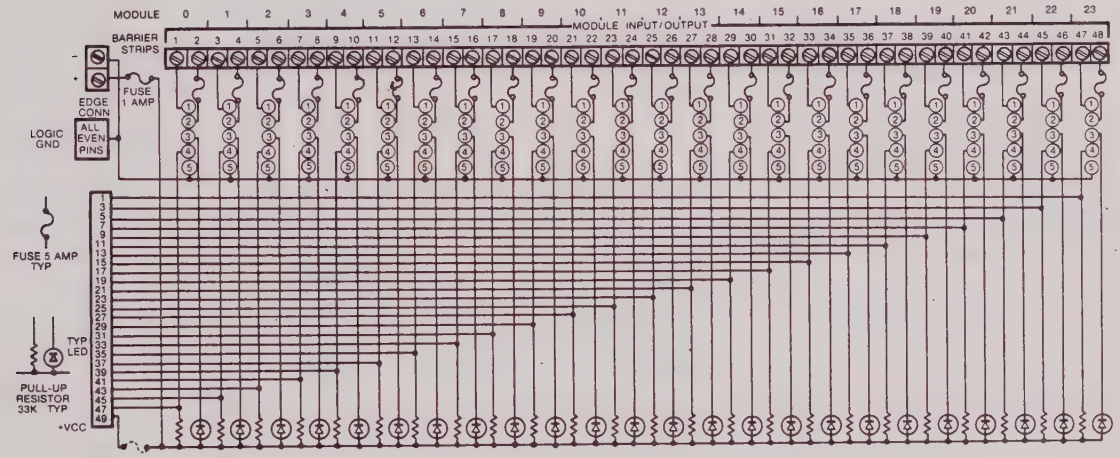


Figure 3-6. Typical I/O Rack Schematic

USING BIDIRECTIONAL SIGNAL LINES

The schematic of a typical bidirectional line in the interface card is shown in figure 3-7. It consists of an output latch, output buffer, input gate, and LED indicators on MOD 0, 1, and 2.

As an input line, the associated output line must be in the inactive (high) state. The output ports are in the inactive state after power-up or pushbutton reset. Ensure that the output of any bidirectional line being used as an input remains in the inactive state at all times. Whenever writing to a port being used partly as input and partly as output, zeros should be written to the lines being used as inputs.

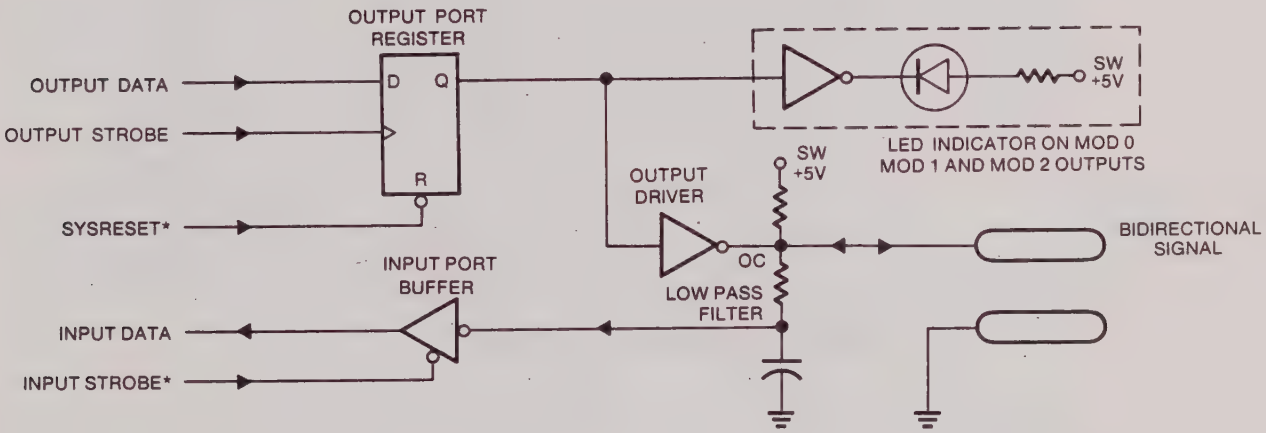


Figure 3-7. Typical Bidirectional I/O Circuit (7507)

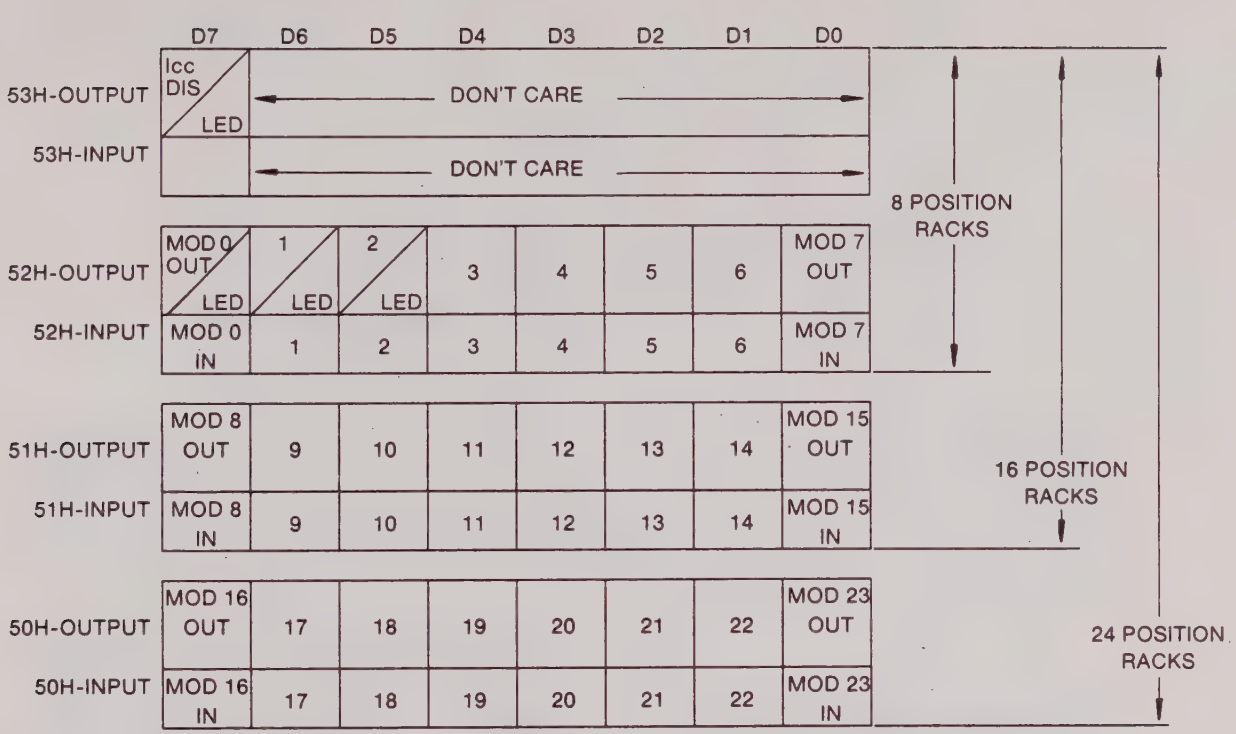


Figure 3-8. Port Mapping (7507)

I/O RACK POWER LINE

> **CAUTION**
>
> There is no current limiting on this line, so take care not to short it to ground. Connecting the cable backward may short this line to ground. Therefore, key the connectors to avoid this possibility. Both the interface card and the I/O rack have slots in their card edges for keyed connectors.

The I/O rack requires a +5V supply. The I/O rack has a two-position terminal block to which power can be connected directly or power can be supplied through the interface card. Line 49 of the interface card provides up to 500 mA at 4.75V. It can be controlled via software or permanently connected directly to the +5V supply of the STD card rack. (See section 2, Module Rack Power, page 2-5.)

Software control of the I/O rack power line can be used to turn off the entire I/O rack, which may be useful in emergency situations.

Port 53, data bit 7, is used to control the I/O rack power line (see figure 3-8). Power is on after power-up or pushbutton reset, and a one must be written to this bit to turn power off.

Power must be applied to the rack for a self-test that writes to an output port and reads back at an input port. This is because the pullups for the open-collector output drivers are connected to the switched +5V. This switched power at the pull-ups eliminates a possible sneak current path through the pull-ups and a nonpowered rack.

LED INDICATORS

There are four LEDs on the interface card above the interface connector (see figure 2-2, page 2-2). LEDs 0, 1, and 2 correspond to modules 0, 1, and 2. These LEDs are on when the output is active high. LED 3 is associated with the I/O rack power line. It is lit when power is on. After power-up or pushbutton reset, LEDs 0, 1, and 2 will be off, LED 3 will be on.

GENERAL PURPOSE USE

The interface card can be used as a general purpose I/O card. The alternating signal and ground lines plus the filtering on the input ports offers a high degree of noise immunity in an I/O card. When using the interface card for general purpose work, be sure to take into account the 15 microsecond delay of the input filters.

SERIES 90 PROM PROGRAMMER INTERFACE

Pro-Log offers the PIN 114 parallel interface option for communication between an STD BUS system and a Pro-Log Series 90 PROM Programmer. The PIN 114 is based on the interface card. Software to operate the interface is resident in Pro-Log's MP4 and MP5 monitor programs. For more information on the PIN 114, see appendix A at the back of this manual.

INTRODUCTION

This section contains hardware-level subroutine modules to operate the I/O rack interface card.

The software in this section may be used without license from Pro-Log. Although tested and believed to be correct, this software is not represented to be free from errors, copyright infringement, or appropriate for any particular application.

These subroutines are written in STD instruction mnemonics. The coding forms are grouped at the end of this section. Individual subroutine specifications show memory requirements, entry requirements, and exit characteristics for each path in the program. Timing and other necessary information are also provided.

MEMORY ADDRESSES

Full memory addresses are shown in the subroutine documentation. They are the preferred addresses that allow the subroutines to work with those provided for other Series 7000 STD BUS cards.

If your system cannot use the memory addresses in the following software package, simply change the memory page addresses as required. Memory addresses that must be located in RAM are noted on the program coding forms. Other memory addresses shown are intended to be ROM locations, but may be RAM locations.

I/O PORT ADDRESSES

The interface card I/O ports are assigned preferred addresses 50H through 53H for compatibility with other Series 7000 cards. Section 2 shows how to remap these addresses if necessary. This software can be used by simply changing the port addresses when loading the subroutines into your system.

SOFTWARE PACKAGE CONTENTS

The software package listed here can be used to drive a standard I/O module mounting rack. To drive an addressed I/O module mounting rack (such as the Adatek RP32), consult the manufacturer of the mounting rack.

Figure 4-1 lists the general purpose hardware-level subroutines provided to operate the interface card. These subroutines allow the card to communicate with the I/O module mounting rack on a bit-by-bit basis. With this software approach, you can turn on, turn off, or check the status of any one device without affecting any of the other devices connected to the I/O module mounting rack.

MODULE NAME	SUBROUTINE FUNCTION	SEE FIGURE
(INITIALIZE)	This subroutine sets all outputs to a predefined state. It also initializes all variables used by the other subroutines.	4-4 4-5 4-6
(COMPLEMENT A BIT)	This subroutine complements one bit of the output lines.	4-7 4-8 4-9 4-10 4-11
(SET A BIT)	This subroutine sets one bit of the output lines.	4-12 4-13 4-14 4-15 4-16
(CLEAR A BIT)	This subroutine clears one bit of the output lines.	4-17 4-18 4-19 4-20 4-21
(TEST A BIT)	This subroutine checks the state of one of the output lines.	4-22 4-23 4-24 4-25 4-26
(TEST INPUT BIT)	This subroutine checks the state of one of the input lines.	4-27 4-28 4-29 4-30 4-31
(PWR ON)	Turns on module rack power.	4-32 4-33 4-34
(PWR OFF)	Turns off module rack power.	4-35 4-36 4-37
(WHICH LINE?)	This subroutine is used by the other subroutines to find the Port and Bit of the desired module.	4-38 4-39 4-40

Figure 4-1. Index of Subroutines (7507)

MEMORY MAPS

Figure 4-2 is a 16K memory map that shows the location of the software package.

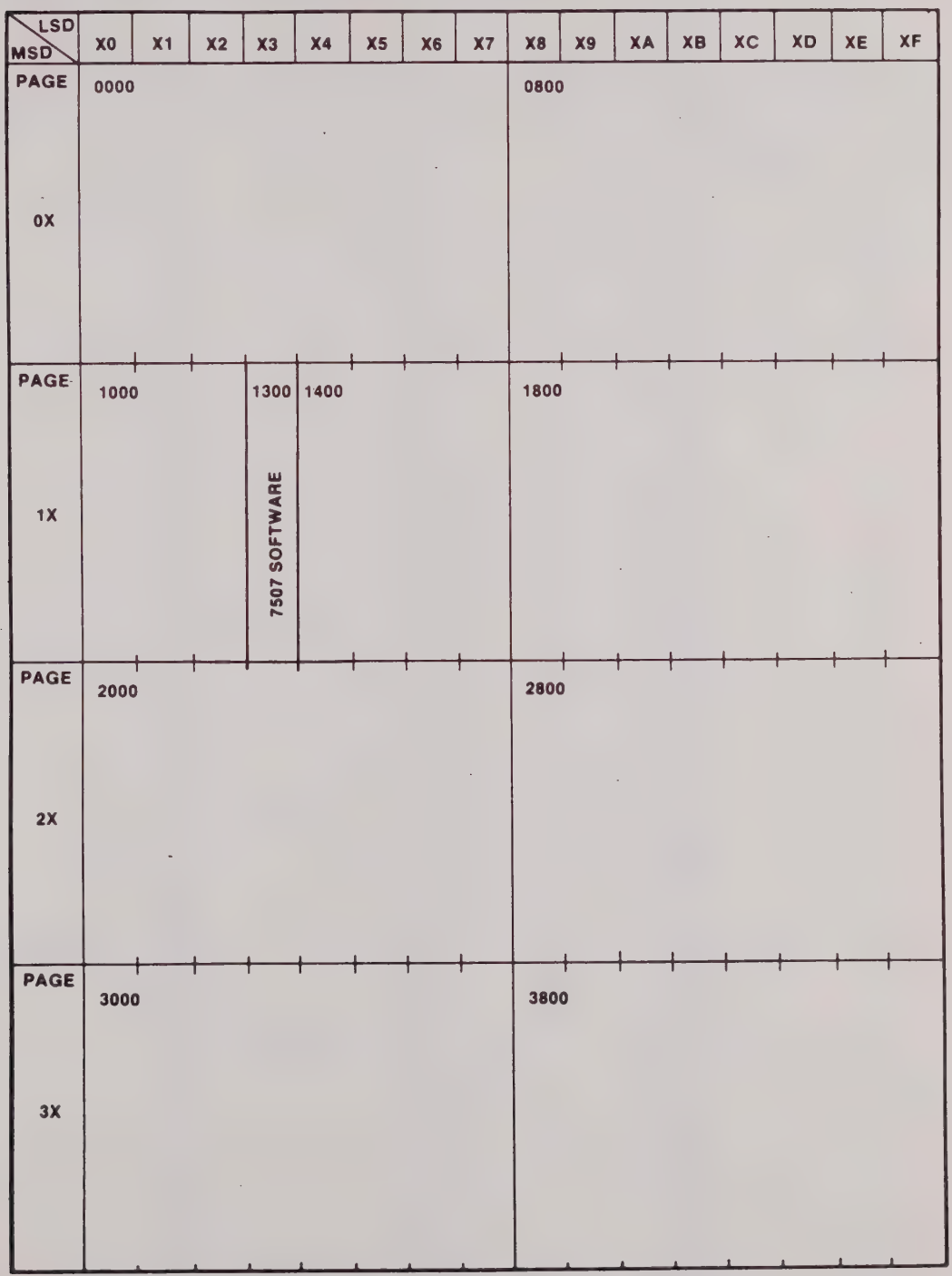


Figure 4-2. Software Package Locations (7507)

Figure 4-3 is a page map that shows subroutine locations.

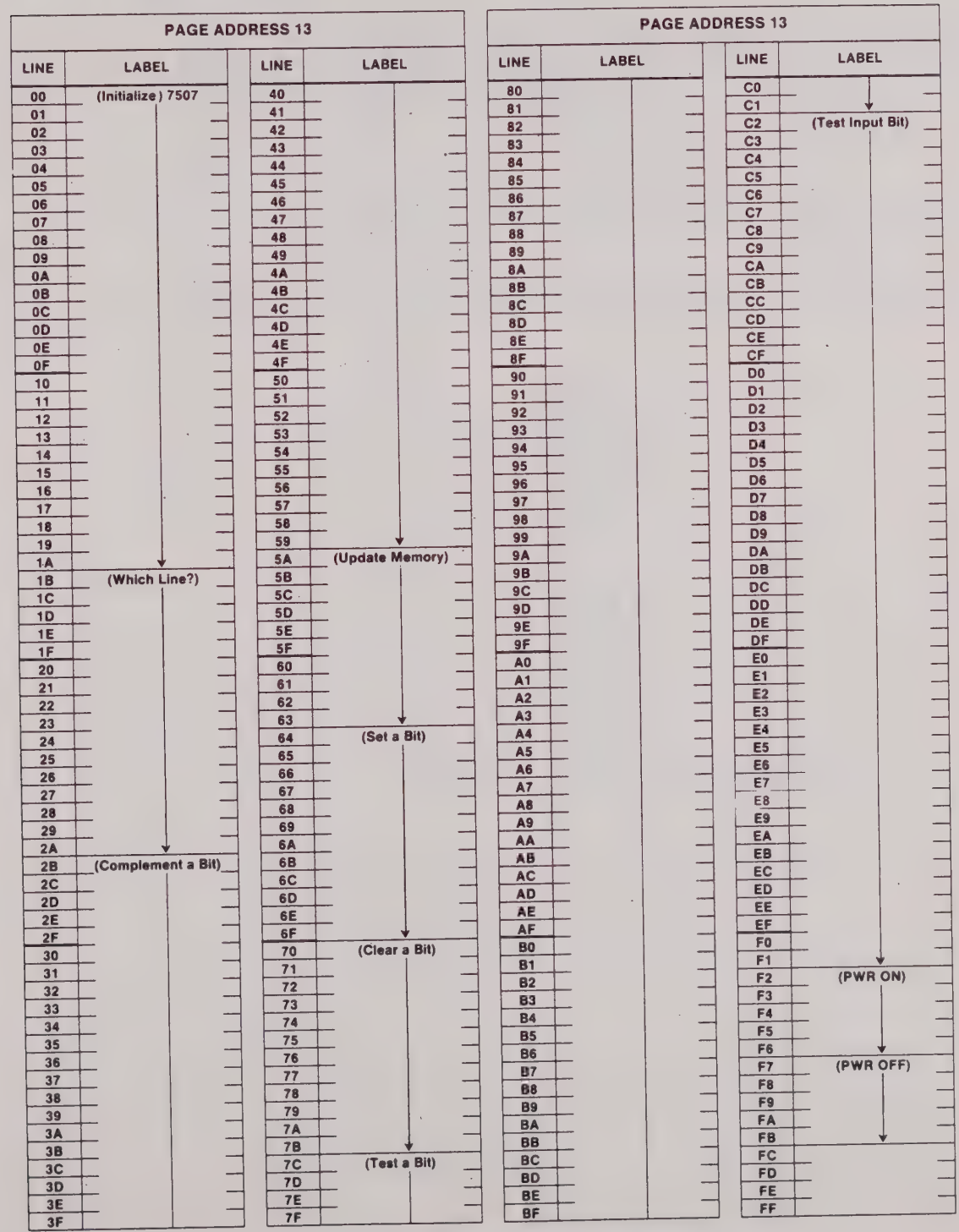


Figure 4-3. Subroutine Locations (7507)

(INITIALIZE) SUBROUTINE

This subroutine sets all outputs to a predefined state. It also initializes all variables used by the other subroutines.

To use this routine:

1. Select three consecutive memory locations in RAM memory and put the first address in locations 1301 and 1302. These three RAM locations are used by the other subroutines in this package.

2. Put the initial state of modules 16-23 into location 1304H (D0=MOD23, D7=MOD 16).

3. Put the initial state of modules 8-15 into location 1308H (D0=MOD 15, D7=MOD 8).

4. Put the initial state of modules 0-7 into location 130CH (D0=MOD 7, D7=MOD 0).

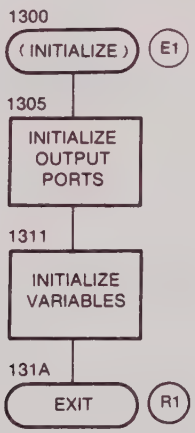


Figure 4-4. Initialization Flowchart

PARAMETER		ENTRY E1	RETURN R1	COMMENT
ELEMENT	ADDRESS			
Register	A	XX	??	Logic states of module 0-7
Register	H	XX	RAM Address +2	Last location of the three RAM storage locations.
Register	L			
Memory	1301	RAM Address	RAM Address +2	First location of the three RAM storage locations.
Memory	1302			
Memory	1304	D7=MOD 16, D0=MOD 23	D7=MOD 16, D0=MOD 23	Port 0 Initial state.
Memory	1308	D7=MOD 8, D0=MOD 15	D7=MOD 8, D0=MOD 15	Port 1 Initial state.
Memory	130C	D7=MOD 0, D0=MOD 7	D7=MOD 0, D0=MOD 7	Port 2 Initial state.

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-5. Register and Memory Allocation for (INITIALIZE) Subroutine

SYMBOL	SUBROUTINE PARAMETER		RETURN			UNITS
			MIN		MAX	
Ns	Stack Memory			2		Bytes
Np	Program Memory			27		Bytes
Npt	Total Program Memory			27		Bytes
Nr	RAM Memory			3		Bytes
Te	Execution Time	8085		134		Time States
		Z80		140		

NOTES:
1 Stack Memory includes return address

Figure 4-6. Characteristics of (INITIALIZE) Subroutine

(COMPLEMENT A BIT) SUBROUTINE

This routine accepts a hex value in the accumulator. This value corresponds to the I/O module to be complemented. If the I/O module number is out of range, the carry flag is set.

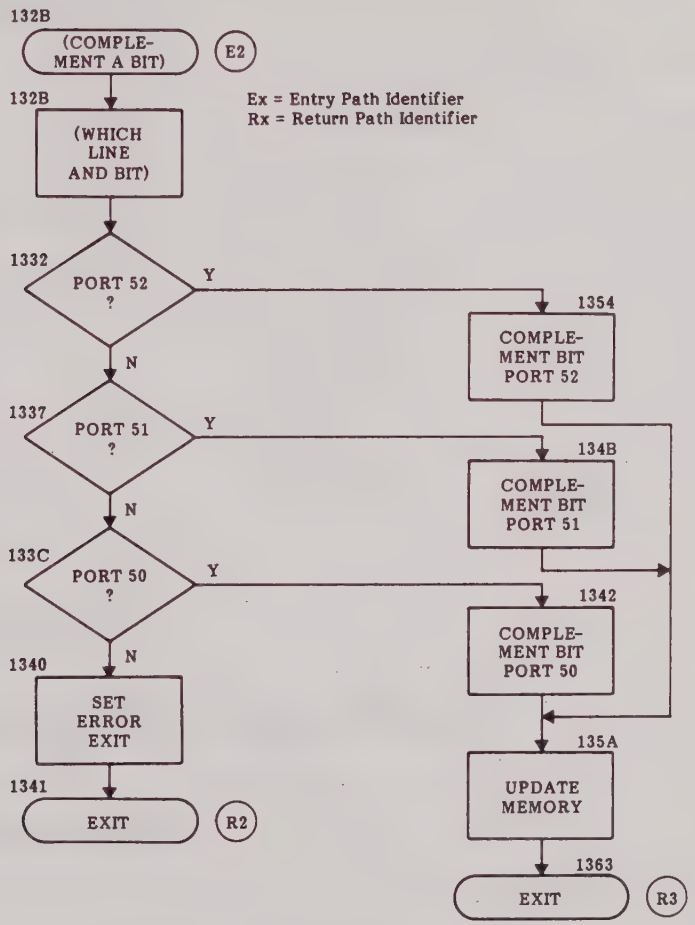


Figure 4-7. (COMPLEMENT A BIT) Flowchart

If this routine returns with an error condition, use figures 4-8 and 4-9. An error condition indicates that the module number was too high. Alternately, in systems with more than 24 modules, this return condition could be used as a flag for jumping to the second interface card's software.

PARAMETER		ENTRY E2	RETURN R2	COMMENT
ELEMENT	ADDRESS			
Register	A	Module Number	??	—
Register	B	XX	Port Number -3	See (WHICH LINE?)
Register	C	XX	00	—
Register	H	XX	RAM Address +2	First location of the three RAM storage locations.
Register	L			
Register	F	XX	Carry=1	ERROR FLAG—
Memory	132F	RAM Address +2	RAM Address +2	Last location of the three RAM storage locations.
Memory	1330			

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-8. Register and Memory Allocation for (COMPLEMENT A BIT) Subroutine Return 2

SYMBOL	SUBROUTINE PARAMETER		RETURN MIN	RETURN	RETURN MAX	UNITS
Ns	Stack Memory[1]			4		Bytes
Np	Program Memory			23		Bytes
Npt	Total Program Memory			39		Bytes
Nr	RAM Memory			3		Bytes
Te	Execution Time	8085		—		Time States
		Z80		—		

NOTES:
[1] Stack Memory includes return address.

Figure 4-9. Characteristics of (COMPLEMENT A BIT) Subroutine Return 2

If this routine returns without error, use figures 4-10 and 4-11.

PARAMETER		ENTRY E2	RETURN R3	COMMENT
ELEMENT	ADDRESS			
Register	A	Module Number	??	—
Register	B	XX	00	—
Register	C	XX	00	—
Register	H	XX	Memory Pointer	—
Register	L			
Register	F	XX	Carry=0	NO ERROR
RAM (HL)		Before DATA	After DATA	—
Memory	132F	RAM Address +2	RAM Address +2	Last location of the three RAM storage locations
Memory	1330			

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-10. Register and Memory Allocation for (COMPLEMENT A BIT) Subroutine Return 3

SYMBOL	SUBROUTINE PARAMETER		RETURN MIN		RETURN MAX	UNITS
Ns	Stack Memory[1]			4		Bytes
Np	Program Memory			57		Bytes
Npt	Total Program Memory			73		Bytes
Nr	RAM Memory			3		Bytes
Te	Execution Time[2,3,4,5]	8085	160		740	Time States
		Z80	160		730	

NOTES:
[1] Stack Memory includes return address
[2] Subroutine call not included in execution time.
[3] Assumes a 24-module rack; MIN for Module 0, MAX for module 23.
[4] 8085 time states = 122 + (WHICH LINE?) +27 (if module #8) +1 (if module #16).
[5] Z80 time states = 123 + (WHICH LINE?) +32 (if module #8) +18 (if module #16).

Figure 4-11. Characteristics of (COMPLEMENT A BIT) Subroutine Return 3

(SET A BIT) SUBROUTINE

This routine accepts a hex value in the accumulator. This value corresponds to the I/O module to be turned on. If the I/O module number is out of range, the carry flag is set.

If this routine returns with an error condition, use figures 4-13 and 4-14. An error condition indicates that the module number was too high. Alternately, in systems with more than 24 modules, this return condition could be used as a flag for jumping to an extension of this routine to accommodate more modules.

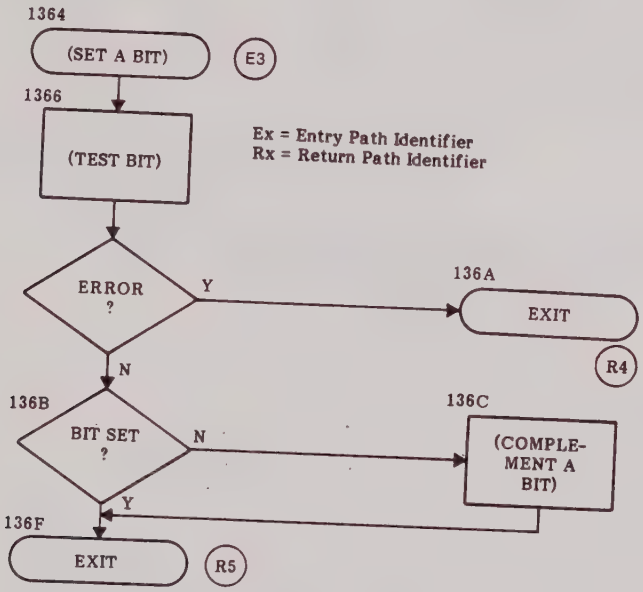


Figure 4-12. (SET A BIT) Flowchart

PARAMETER		ENTRY E3	RETURN R4	COMMENT
ELEMENT	ADDRESS			
Register	A	Module Number	??	—
Register	B	XX	Port Number -3	See (WHICH LINE?)
Register	C	XX		—
Register	H	XX	RAM Address +2	First location of the three RAM storage locations.
Register	L			
Register	F	XX	Carry = 1	ERROR FLAG

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-13. Register and Memory Allocation for (SET A BIT) Subroutine Return 4

SYMBOL	SUBROUTINE PARAMETER		RETURN			UNITS
			MIN		MAX	
Ns	Stack Memory[1]			6		Bytes
Np	Program Memory			30		Bytes
Npt	Total Program Memory			46		Bytes
Nr	RAM Memory			0		Bytes
Te	Execution Time	8085		—		Time States
		Z80		—		

OTES:
Stack Memory includes return address.

Figure 4-14. Characteristics of (SET A BIT) Subroutine Return 4

If this routine returns without error, use figures 4-15 and 4-16.

PARAMETER		ENTRY E3	RETURN R5	COMMENT
ELEMENT	ADDRESS			
Register	A	Module Number	??	—
Register	B	XX	00	—
Register	C	XX	00	—
Register	H	XX	Memory Pointer	—
Register	L			
Register	F	XX	Carry = 0	NO ERROR
RAM (HL)		Before DATA	After DATA	—
Memory	132F	RAM Address +2	RAM Address +2	Last location of the three RAM storage locations
Memory	1330			

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-15. Register and Memory Allocation for (SET A BIT) Subroutine Return 5

SYMBOL	SUBROUTINE PARAMETER		RETURN MIN		RETURN MAX	UNITS
Ns	Stack Memory[1]			6		Bytes
Np	Program Memory			12		Bytes
Npt	Total Program Memory			85		Bytes
Nr	RAM Memory			3		Bytes
Te_1	Execution Time[2,3,4,5]	8085	408		998	Time States
	Bit previously set	Z80	399		976	
Te_2	Execution Time[2,3,6,7]	8085	577		1738	Time States
	Bit previously set	Z80	566		1706	

NOTES:
[1] Stack Memory includes return address.
[2] Subroutine call not included in execution time.
[3] Assumes a 24-module rack; MIN for Module 0, MAX for module 23.
[4] 8085 time states = 73 + (TEST A BIT).
[5] Z80 time states = 71 + (TEST A BIT).
[6] 8085 time states = 82 + (TEST A BIT) + (COMPLEMENT A BIT).
[7] Z80 time states = 78 + (TEST A BIT) + (COMPLEMENT A BIT).

Figure 4-16. Characteristics of (SET A BIT) Subroutine Return 5

(CLEAR A BIT) SUBROUTINE

This routine accepts a hex value in the accumulator. This value corresponds to the I/O module to be turned off. If the I/O module number is out of range, the carry flag is set.

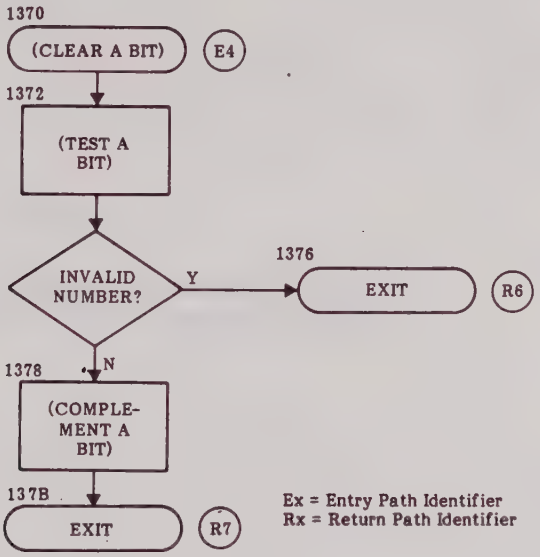


Figure 4-17. (CLEAR A BIT) Flowchart

If this routine returns with an error condition, use figures 4-18 and 4-19. An error condition indicates that the module number was too high. Alternately, in systems with more than 24 modules, this return condition could be used as a flag for jumping to an extension of this routine which could accommodate additional modules.

PARAMETER		ENTRY E4	RETURN R6	COMMENT
ELEMENT	ADDRESS			
Register	A	Module Number	??	—
Register	B	XX	Port Number	See (WHICH LINE?)
Register	C	XX	??	—
Register	H	XX	RAM Address	First location of the three RAM storage locations.
Register	L			
Register	F	XX	Carry = 1	ERROR FLAG

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-18. Register and Memory Allocation for (CLEAR A BIT) Subroutine Return 6

SYMBOL	SUBROUTINE PARAMETER		RETURN			UNITS
			MIN		MAX	
Ns	Stack Memory[1]			6		Bytes
Np	Program Memory			30		Bytes
Npt	Total Program Memory			46		Bytes
Nr	RAM Memory			0		Bytes
Te	Execution Time	8085		—		Time States
		Z80		—		

NOTES:
[1] Stack Memory includes return address.

Figure 4-19. Characteristics of (CLEAR A BIT) Subroutine Return 6

If this routine returns without error, use figures 4-20 and 4-21.

PARAMETER		ENTRY E3	RETURN R7	COMMENT
ELEMENT	ADDRESS			
Register	A	Module Number	??	—
Register	B	XX	??	—
Register	C	XX	??	—
Register	H	XX	Memory Pointer	—
Register	L			
Register	F	XX	Carry = 0	NO ERROR
RAM (HL)		Before DATA	After DATA	—
Memory	132F	RAM Address +2	RAM Address +2	Last location of the three RAM storage locations.
Memory	1330			

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-20. Register and Memory Allocation for (CLEAR A BIT) Subroutine Return 7

SYMBOL	SUBROUTINE PARAMETER		RETURN MIN		RETURN MAX	UNITS
Ns	Stack Memory[1]			6		Bytes
Np	Program Memory			12		Bytes
Npt	Total Program Memory			85		Bytes
Nr	RAM Memory			3		Bytes
Te_1	Execution Time[2,3,4,5]	8085	408		998	Time States
	Bit previously set	Z80	399		976	
Te_2	Execution Time[2,3,6,7]	8085	577		1738	Time States
	Bit previously clear	Z80	566		1706	

NOTES:
1. Stack Memory includes return address.
2. Subroutine call not included in execution time.
3. Assumes a 24-module rack; MIN for Module 0, MAX for module 23.
4. 8085 time states = 73 + (TEST A BIT).
5. Z80 time states = 71 + (TEST A BIT).
6. 8085 time states = 82 + (TEST A BIT) + (COMPLEMENT A BIT).
7. Z80 time states = 78 + (TEST A BIT) + (COMPLEMENT A BIT).

Figure 4-21. Characteristics of (CLEAR A BIT) Subroutine Return 7

(TEST A BIT) SUBROUTINE

The (TEST A BIT) subroutine is used to check the state of an output module. It is also used by the (TEST INPUT MODULE) subroutine. (TEST A BIT) accepts a hex value in the accumulator. This value corresponds to the output module to be tested. If the I/O module number is out of range, the carry flag is set. It returns with the sign flag=0 if there was no change and S=1 if the addressed module has changed since the last test. The Z flag equals zero if the bit is set and Z equals one if the input bit is clear.

If this routine returns with an error condition, use figures 4-23 and 4-24. An error condition indicates that the module number was too high. Alternately, in systems with more than 24 modules, this return condition could be used as a flag for jumping to an extension of this software that could accommodate more modules.

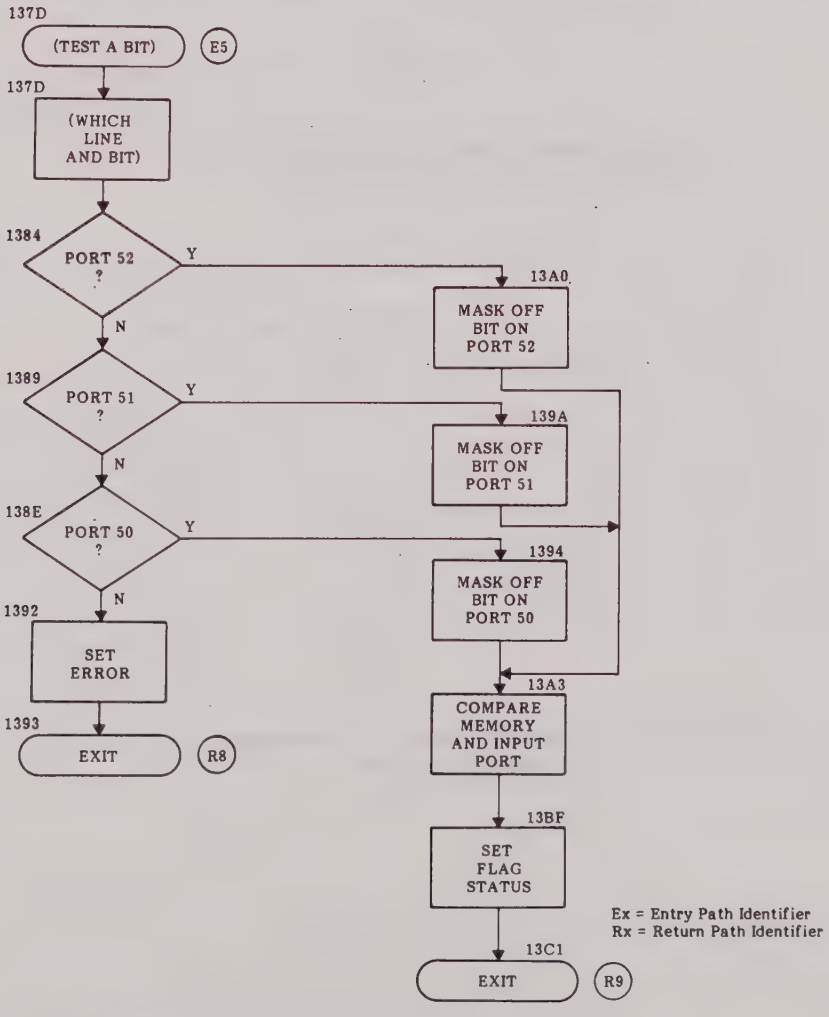


Figure 4-22. (TEST A BIT) Flowchart

PARAMETER		ENTRY E5	RETURN R8	COMMENT
ELEMENT	ADDRESS			
Register	A	Module Number	??	—
Register	B	XX	Port Number	See (WHICH LINE?)
Register	C	XX	??	—
Register	H	XX	RAM Address	First location of the three RAM storage locations.
Register	L			
Register	F	XX	Carry = 1	ERROR FLAG
Memory	132F	RAM Address +2	RAM Address +2	Last location of the three RAM storage locations.
Memory	1330			

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-23. Register and Memory Allocation for (TEST A BIT) Subroutine Return 8

SYMBOL	SUBROUTINE PARAMETER		RETURN MIN		RETURN MAX	UNITS
Ns	Stack Memory[1]			4		Bytes
Np	Program Memory			23		Bytes
Npt	Total Program Memory			39		Bytes
Nr	RAM Memory			3		Bytes
Te	Execution Time	8085		—		Time States
		Z80		—		

NOTES:
[1] Stack Memory includes return address.

Figure 4-24. Characteristics of (TEST A BIT) Subroutine Return 8

If this routine returns with an error condition, use figures 4-28 and 4-29. An error condition indicates that the module number was too high. Alternately, in systems with more than 24 modules, this return condition could be used as a flag for jumping to an extension of this routine to accommodate more modules.

PARAMETER		ENTRY E6	RETURN R10	COMMENT
ELEMENT	ADDRESS			
Register	A	Module Number	??	—
Register	B	XX	Port Number -3	See (WHICH LINE?)
Register	C	XX	00	—
Register	H	XX	RAM Address	First location of the three RAM storage locations.
Register	L			
Register	F	XX	Carry = 1	ERROR FLAG
Memory		RAM Address +2	RAM Address +2	Last location of the three RAM storage locations.
Memory				

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-28. Register and Memory Allocation for (TEST INPUT BIT) Subroutine Return 10

SYMBOL	SUBROUTINE PARAMETER		RETURN MIN		RETURN MAX	UNITS
Ns	Stack Memory[1]			4		Bytes
Np	Program Memory			23		Bytes
Npt	Total Program Memory			39		Bytes
Nr	RAM Memory			3		Bytes
Te	Execution Time	8085		—		Time States
		Z80		—		

NOTES:
[1] Stack Memory includes return address

Figure 4-29. Characteristics of (TEST INPUT BIT) Subroutine Return 10

If this routine returns without error, use figures 4-30 and 4-31.

PARAMETER		ENTRY E6	RETURN R11	COMMENT
ELEMENT	ADDRESS			
Register	A	Module Number	??	—
Register	B	XX	??	—
Register	C	XX	??	—
Register	H	XX	Memory Pointer	—
Register	L			
Register	F	XX	Carry = 0	NO ERROR
RAM (HL)		Before DATA	After DATA	—
Memory	1381	RAM Address +2	RAM Address +2	Last location of the three RAM storage locations.
Memory	1382			

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-30. Register and Memory Allocation for (TEST INPUT BIT) Subroutine Return 11

SYMBOL	SUBROUTINE PARAMETER		RETURN MIN		RETURN MAX	UNITS
Ns	Stack Memory[1]			4		Bytes
Np	Program Memory			48		Bytes
Npt	Total Program Memory			146		Bytes
Nr	RAM Memory			3		Bytes
Te	Execution Time[2,3,4,5]	8085	445		1594	Time States
	Bit previously set	Z80	436		1504	

NOTES:
[1] Stack Memory includes return address.
[2] Subroutine call not included in execution time.
[3] Assumes a 24-module rack; MIN for Module 0, MAX for module 23.
[4] 8085 time states = 72 + (WHICH LINE?) + (TEST A BIT) + 27 (if module #8) + 11 (if module #16).
[5] Z80 time states = 71 + (WHICH LINE?) + (TEST A BIT) + 24 (if module #8) + 14 (if module #16).

Figure 4-31. Characteristics of (TEST INPUT BIT) Subroutine Return 11

(PWR ON) SUBROUTINE

This routine turns on the power to the I/O module rack.

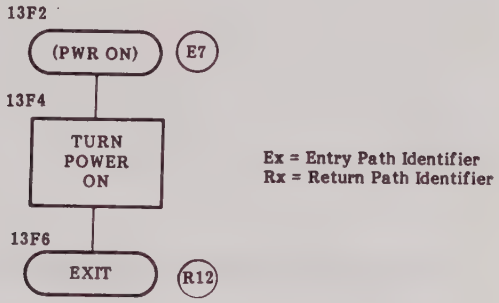


Figure 4-32. (PWR ON) Flowchart

PARAMETER		ENTRY E7	RETURN R12	COMMENT
ELEMENT	ADDRESS			
Register	A	XX	00	—

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.

Figure 4-33. Register and Memory Allocation for (PWR ON) Subroutine

SYMBOL	SUBROUTINE PARAMETER		RETURN			UNITS
			MIN		MAX	
Ns	Stack Memory[1]			2		Bytes
Np	Program Memory			5		Bytes
Npt	Total Program Memory			5		Bytes
Nr	RAM Memory			0		Bytes
Te	Execution Time	8085		27		Time States
		Z80		28		

NOTES:
[1] Stack Memory includes return address.

Figure 4-34. Characteristics of (PWR ON) Subroutine

(PWR OFF) SUBROUTINE

This routine turns off the power to the I/O module rack.

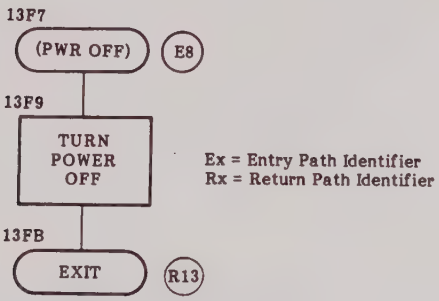


Figure 4-35. (PWR OFF) Flowchart

PARAMETER		ENTRY E8	RETURN R13	COMMENT
ELEMENT	ADDRESS			
Register	A	XX	00	—

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.

Figure 4-36. Register and Memory Allocation for (PWR OFF) Subroutine

SYMBOL	SUBROUTINE PARAMETER		RETURN			UNITS
			MIN		MAX	
Ns	Stack Memory[1]			2		Bytes
Np	Program Memory			5		Bytes
Npt	Total Program Memory			5		Bytes
Nr	RAM Memory			0		Bytes
Te	Execution Time	8085		27		Time States
		Z80		28		

NOTES:
[1] Stack Memory includes return address.

Figure 4-37. Characteristics of (PWR OFF) Subroutine

(WHICH LINE?) SUBROUTINE

This is a support routine used by other routines to calculate the correct port and bit for each module. The routine can be used alone for other purposes. It converts a number in the accumulator into the correct port and bit numbers. This routine is not limited to the 24-position rack; it can calculate the correct port and bit for up to 256 modules.

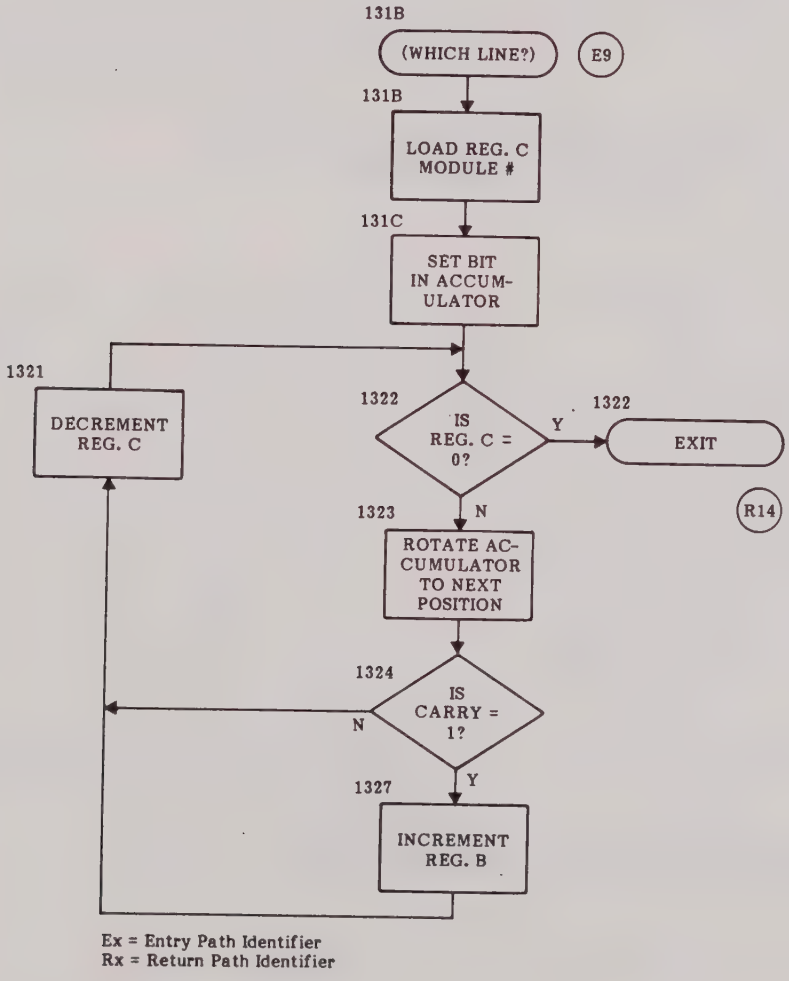


Figure 4-38. (WHICH LINE?) Flowchart

PARAMETER		ENTRY E9	RETURN R14	COMMENT
ELEMENT	ADDRESS			
Register	A	Module Number	Which Bit	—
Register	B	XX	Port Number	1 = Port 0, 2 = Port 1, etc.
Register	C	XX	00	—
Register	F	XX	Z = 1	—

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-39. Register and Memory Allocation for (WHICH LINE?) Subroutine

SYMBOL	SUBROUTINE PARAMETER		RETURN MIN		RETURN MAX	UNITS
Ns	Stack Memory[1]			2		Bytes
Np	Program Memory			16		Bytes
Npt	Total Program Memory			16		Bytes
Nr	RAM Memory			0		Bytes
Te	Execution Time[2,3,4,5]	8085	38		574	Time States
	Bit previously set	Z80	37		557	

NOTES:
[1] Stack Memory includes return address.
[2] Subroutine call not included in execution time.
[3] Assumes a 24-module rack; MIN for Module 0, MAX for module 23.
[4] 8085 time states = 38 + 24 (per module #) + 11 (every eighth module).
[5] Z80 time states = 37 + 23 (per module #) + 14 (every eighth module).

Figure 4-40. Characteristics of (WHICH LINE?) Subroutine

```
ADRdata!     LABEL          !INSTR !    MODIFIER    !            COMMENTS
-------------------------------------------------------------------------------
1300 21!(INIT 7507)         !LDPI  !HL              !*INITIALIZE PROGRAM
  01 __!                    ! ---- !RAM PAGE        !
  02 __!                    ! ---- !                !
  03 3E!                    !LDAI  !                !Set port 50
  04 __!                    ! ---- !deleted label   !
  05 D3!                    !OPA   !                !
  06 50!                    ! ---- !50 hex          !
  07 3E!                    !LDAI  !                !Set port 51
  08 __!                    ! ---- !deleted label   !
  09 D3!                    !OPA   !                !
  0A 51!                    ! ---- !51 hex          !
  0B 3E!                    !LDAI  !                !Set port 52
  0C __!                    ! ---- !deleted label   !
  0D D3!                    !OPA   !                !
  0E 52!                    ! ---- !52 hex          !
  0F DB!                    !IPA   !                !Set memory to I/O port status
1310 50!                    ! ---- !50 hex          !
  11 77!                    !STAN  !(HL)            !
  12 23!                    !ICP   !HL              !
  13 DB!                    !IPA   !                !
  14 51!                    ! ---- !51 hex          !
  15 77!                    !STAN  !(HL)            !
  16 23!                    !ICP   !HL              !
  17 DB!                    !IPA   !                !
  18 52!                    ! ---- !52 hex          !
  19 77!                    !STAN  !(HL)            !
  1A C9!  ----------        !RTS   !UN              !Return
1B 4F!(WHICH LINE?)         !LDR   !C,A             !*CONVERT MODULE NUMBER TO BIT
  1C 3E!                    !LDAI  !                !    POSITION
  1D 80!                    ! ---- !80 hex          !    Bit=A, port=B
  1E 06!                    !LDRI  !B               !
  1F 01!                    ! ---- !01 hex          !
1320 0C!                    !ICR   !C               !Increment "C"
1321 0D!LOOP                !DCR   !C               !Decrement "C"
  22 C8!                    !RTS   !ZERO            !Return when zero
  23 0F!                    !RRA   !                !Next bit position
  24 D2!                    !JP    !NO CARRY        !
  25 21!                    ! ---- !LOOP            !
  26 13!                    ! ---- !                !
  27 04!                    !ICR   !B               !Increment "B" until C flag set
  28 C3!                    !JP    !UN              !
  29 21!                    ! ---- !LOOP            !
  2A 13!  ----------        ! ---- !                !
2B CD!(COMPLEMENT BIT)      !JS    !UN              !*CHANGE STATE OF SELECTED
  2C 1B!                    ! ---- !(WHICH LINE?)   !    MODULE
  2D 13!                    ! ---- !                !
  2E 21!                    !LDPI  !HL              !Set pointer to last port
  2F __!                    ! ---- !RAM PAGE        !
1330 __!                    ! ---- !                !
  31 05!                    !DCR   !B               !Find correct port routine
  32 CA!                    !JP    !ZERO            !
  33 54!                    ! ---- !PORT 52 A       !
  34 13!                    ! ---- !                !
  35 2B!                    !DCP   !HL              !
  36 05!                    !DCR   !B               !
  37 CA!                    !JP    !ZERO            !
  38 4B!                    ! ---- !PORT 51 A       !
  39 13!                    ! ---- !                !
  3A 2B!                    !DCP   !HL              !
  3B 05!                    !DCR   !B               !
  3C CA!                    !JP    !ZERO            !
  3D 42!                    ! ---- !PORT 50 A       !
  3E 13!                    ! ---- !                !
  3F 00!                    !NOP   !                !
```

Figure 4-41. Program Listing for Subroutines

```
ADRdata!      LABEL       !INSTR !    MODIFIER    !            COMMENTS
-------------------------------------------------------------------------------
1340 37!                  !SEC   !                !
  41 C9!   ----------     !RTS   !UN              !Return. C=1 if invalid number
1342 47!PORT 50 A         !LDR   !B,A             !Update port 50
  43 DB!                  !IPA   !                !
  44 50!                  ! ---- !50 hex          !
  45 A8!                  !XRA   !B               !
  46 D3!                  !OPA   !                !
  47 50!                  ! ---- !50 hex          !
  48 C3!                  !JP    !UN              !
  49 5A!                  ! ---- !UPDATE MEMORY   !
  4A 13!   ----------     ! ---- !                !
134B 47!PORT 51 A         !LDR   !B,A             !Update port 51
  4C DB!                  !IPA   !                !
  4D 51!                  ! ---- !51 hex          !
  4E A8!                  !XRA   !B               !
  4F D3!                  !OPA   !                !
1350 51!                  ! ---- !51 hex          !
  51 C3!                  !JP    !UN              !
  52 5A!                  ! ---- !UPDATE MEMORY   !
  53 13!   ----------     ! ---- !                !
1354 47!PORT 52 A         !LDR   !B,A             !Update port 52
  55 DB!                  !IPA   !                !
  56 52!                  ! ---- !52 hex          !
  57 A8!                  !XRA   !B               !
  58 D3!                  !OPA   !                !
  59 52!                  ! ---- !52 hex          !
135A A0!UPDATE MEMORY     !ANA   !B               !Mask all but changed bit
  5B 4F!                  !LDR   !C,A             !Save changed bit in "C"
  5C 78!                  !LDA   !B               !Complement "B" (bit mask)
  5D 2F!                  !CMA   !                !
  5E 47!                  !LDR   !B,A             !
  5F 7E!                  !LDAN  !(HL)            !
1360 A0!                  !ANA   !B               !Mask out changed bit
  61 B1!                  !ORA   !C               !OR in changed bit
  62 77!                  !STAN  !(HL)            !Store new status in memory
  63 C9!   ----------     !RTS   !UN              !Return
1364 47!(SET A BIT)       !LDR   !B,A             !*SET SELECTED MODULE
  65 C5!                  !PSP   !BC              !
  66 CD!                  !JS    !UN              !Check if already set
  67 7D!                  ! ---- !(TEST A BIT)    !
  68 13!                  ! ---- !                !
  69 C1!                  !PLP   !BC              !
  6A D8!                  !RTS   !CARRY           !Return. C=1 if invalid number
  6B 78!                  !LDA   !B               !
  6C CC!                  !JS    !ZERO            !If not set, complement bit
  6D 2B!                  ! ---- !(COMPLEMENT BIT)!
  6E 13!                  ! ---- !                !
  6F C9!   ----------     !RTS   !UN              !Return
1370 47!(CLEAR A BIT)     !LDR   !B,A             !*CLEAR SELECTED MODULE
  71 C5!                  !PSP   !BC              !
  72 CD!                  !JS    !UN              !Check if already clear
  73 7D!                  ! ---- !(TEST A BIT)    !
  74 13!                  ! ---- !                !
  75 C1!                  !PLP   !BC              !
  76 D8!                  !RTS   !CARRY           !Return. C=1 if invalid number
  77 78!                  !LDA   !B               !
  78 C4!                  !JS    !NOT ZERO        !If not clear, complement bit
  79 2B!                  ! ---- !(COMPLEMENT BIT)!
  7A 13!                  ! ---- !                !
  7B C9!   ----------     !RTS   !UN              !Return
  7C FF!                  !      !                !
137D CD!(TEST A BIT)      !JS    !UN              !*CHECK MODULE STATUS
  7E 1B!                  ! ---- !(WHICH LINE?)   !
  7F 13!                  ! ---- !                !
```

Figure 4-41. (Continued)

```
ADRdata!     LABEL       !INSTR !    MODIFIER    !          COMMENTS
-------------------------------------------------------------------------------
1380 21!                 !LDPI  !HL               !Set pointer to last port
  81   !                 ! ---- !RAM PAGE         !
  82   !                 ! ---- !                 !
  83 05!                 !DCR   !B                !Find correct port routine
  84 CA!                 !JP    !ZERO             !
  85 A0!                 ! ---- !PORT 52 B        !
  86 13!                 ! ---- !                 !
  87 2B!                 !DCP   !HL               !
  88 05!                 !DCR   !B                !
  89 CA!                 !JP    !ZERO             !
  8A 9A!                 ! ---- !PORT 51 B        !
  8B 13!                 ! ---- !                 !
  8C 2B!                 !DCP   !HL               !
  8D 05!                 !DCR   !B                !
  8E CA!                 !JP    !ZERO             !
  8F 94!                 ! ---- !PORT 50 B        !
1390 13!                 ! ---- !                 !
  91 00!                 !NOP   !                 !
  92 37!                 !SEC   !                 !
  93 C9!   ----------    !RTS   !UN               !Return. C=1 if invalid number
1394 47!PORT 50 B        !LDR   !B,A              !Save mask
  95 DB!                 !IPA   !                 !Input data
  96 50!                 ! ---- !50 hex           !
  97 C3!                 !JP    !UN               !Update flag status
  98 A3!                 ! ---- !UPDATE FLAGS     !
  99 13!   ----------    ! ---- !                 !
139A 47!PORT 51 B        !LDR   !B,A              !Save mask
  9B DB!                 !IPA   !                 !Input data
  9C 51!                 ! ---- !51 hex           !
  9D C3!                 !JP    !UN               !Update flag status
  9E A3!                 ! ---- !UPDATE FLAGS     !
  9F 13!   ----------    ! ---- !                 !
13A0 47!PORT 52 B        !LDR   !B,A              !Save mask
  A1 DB!   ----------    !IPA   !                 !Input data
  A2 52!                 ! ---- !52 hex           !
13A3 A0!UPDATE FLAGS     !ANA   !B                !Mask unwanted bits (new)
  A4 F5!                 !PSP   !AF               !Save new data and flags
  A5 7E!                 !LDAN  !(HL)             !Load old data
  A6 A0!                 !ANA   !B                !Mask unwanted bits (old)
  A7 4F!                 !LDR   !C,A              !Put old data in "C"
  A8 F1!                 !PLP   !AF               !Set "AF" to new status
  A9 F5!                 !PSP   !AF               !
  AA C5!                 !PSP   !BC               !Save old data
  AB CD!                 !JS    !UN               !Update memory to present status
  AC 5A!                 ! ---- !UPDATE MEMORY    !
  AD 13!                 ! ---- !                 !
  AE C1!                 !PLP   !BC               !Put old data back in "A"
  AF 79!                 !LDA   !C                !
13B0 C1!                 !PLP   !BC               !Put new data and flags in "BC"
  B1 A8!                 !XRA   !B                !XOR old and new data. Z0=change
  B2 F5!                 !PSP   !AF               !Put "change" flag on stack
  B3 79!                 !LDA   !C                !Put zero flag in "A"
  B4 E6!                 !ANAI  !                 !Mask off sign bit
  B5 7F!                 ! ---- !7F hex           !
  B6 C1!                 !PLP   !BC               !Pull "change" flag into "C"
  B7 47!                 !LDR   !B,A              !Put zero flag in "B"
  B8 79!                 !LDA   !C                !Complement "change" flag and
  B9 2F!                 !CMA   !                 !   rotate into sign position
  BA 07!                 !RLA   !                 !
  BB E6!                 !ANAI  !                 !
  BC 80!                 ! ---- !80 hex           !
  BD B0!                 !ORA   !B                !OR "change" and "bit" flags
  BE 4F!                 !LDR   !C,A              !Put flags in "C"
  BF C5!                 !PSP   !BC               !Set flag register
```

Figure 4-41. (Continued)

```
ADRdata!      LABEL       !INSTR !    MODIFIER    !          COMMENTS
-------------------------------------------------------------------------------
13C0 F1!                  !PLP   !AF               !Set flag
  C1 C9!    ----------    !RTS   !UN               !Return
13C2 F5!(TEST INPUT BIT)  !PSP   !AF               !*CHECK INPUT MODULE STATUS
  C3 CD!                  !JS    !UN               !Convert module number to bit
  C4 1B!                  ! ---- !(WHICH LINE?)    !   position
  C5 13!                  ! ---- !                  !
  C6 2F!                  !CMA   !                  !Complement mask
  C7 05!                  !DCR   !B                 !Find port
  C8 CA!                  !JP    !ZERO              !
  C9 E8!                  ! ---- !PORT 52 C         !
  CA 13!                  ! ---- !                  !
  CB 05!                  !DCR   !B                 !
  CC CA!                  !JP    !ZERO              !
  CD DF!                  ! ---- !PORT 51 C         !
  CE 13!                  ! ---- !                  !
  CF 05!                  !DCR   !B                 !
13D0 CA!                  !JP    !ZERO              !
  D1 D6!                  ! ---- !PORT 50 C         !
  D2 13!                  ! ---- !                  !
  D3 F1!                  !PLP   !AF                !
  D4 37!                  !SEC   !                  !
  D5 C9!    ----------    !RTS   !UN               !Return if invalid module. C=1.
13D6 47!PORT 50 C         !LDR   !B,A              !Clear port 50 input module
  D7 DB!                  !IPA   !                  !
  D8 50!                  ! ---- !50 hex            !
  D9 A0!                  !ANA   !B                 !
  DA D3!                  !OPA   !                  !
  DB 50!                  ! ---- !50 hex            !
  DC C3!                  !JP    !UN                !
  DD EE!                  ! ---- !PULL              !
  DE 13!    ----------    ! ---- !                  !
13DF 47!PORT 51 C         !LDR   !B,A              !Clear port 51 input module
13E0 DB!                  !IPA   !                  !
  E1 51!                  ! ---- !51 hex            !
  E2 A0!                  !ANA   !B                 !
  E3 D3!                  !OPA   !                  !
  E4 51!                  ! ---- !51 hex            !
  E5 C3!                  !JP    !UN                !
  E6 EE!                  ! ---- !PULL              !
  E7 13!    ----------    ! ---- !                  !
13E8 47!PORT 52 C         !LDR   !B,A              !Clear port 52 input module
  E9 DB!                  !IPA   !                  !
  EA 52!                  ! ---- !52 hex            !
  EB A0!                  !ANA   !B                 !
  EC D3!                  !OPA   !                  !
  ED 52!                  ! ---- !52 hex            !
13EE F1!PULL              !PLP   !AF               !Restore accumulator
  EF C3!                  !JP    !UN               !Check module status
13F0 7D!                  ! ---- !(TEST A BIT)      !
  F1 13!    ----------    ! ---- !                  !
13F2 3E!(PWR ON)          !LDAI  !                  !*POWER UP MODULE RACK
  F3 00!                  ! ---- !00 hex            !
  F4 D3!                  !OPA   !                  !
  F5 53!                  ! ---- !53 hex            !
  F6 C9!    ----------    !RTS   !UN               !Return
13F7 3E!(PWR OFF)         !LDAI  !                  !*POWER DOWN MODULE RACK
  F8 80!                  ! ---- !80 hex            !
  F9 D3!                  !OPA   !                  !
  FA 53!                  ! ---- !53 hex            !
  FB C9!    ----------    !RTS   !UN               !Return
  FC FF!                  !      !                  !
  FD FF!                  !      !                  !
  FE FF!                  !      !                  !
  FF FF!                  !      !                  !
```

Figure 4-41. (Continued)

INTRODUCTION

This section contains an overview of the interface card circuitry, return for repair procedures, and the two-year limited warranty. The schematic and assembly drawings are located at the back of this manual.

OVERVIEW OF OPERATING CIRCUITS

Card Select

SW controls the state of IOEXP which enables 74LS138s (the card select chips). This card is selected by decoding address lines A2-A7. The decoded address line is then ANDed with the IORQ* signal so the card is selected only during I/O instructions. SX and SY jumper out the proper select signals.

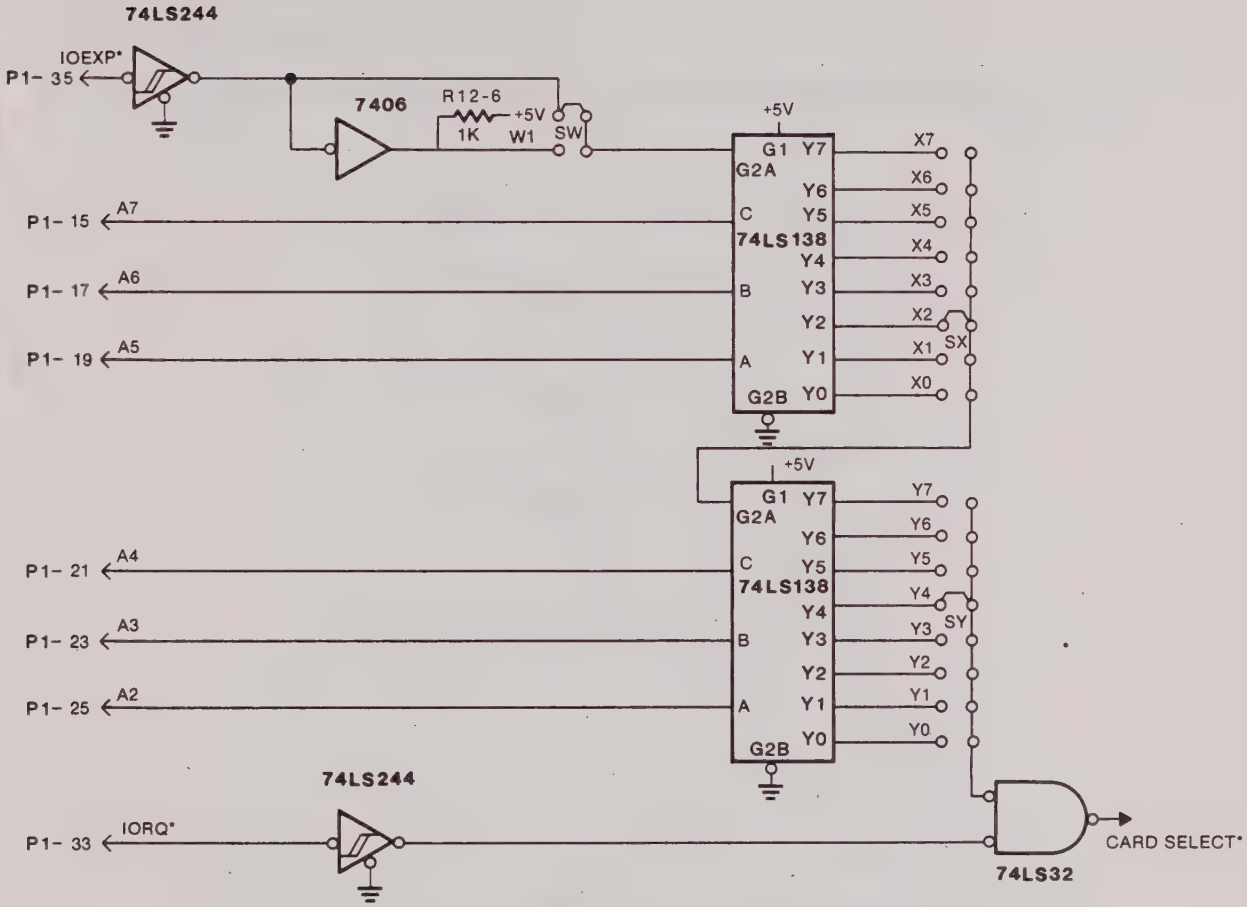


Figure 5-1. Card Select (7507)

Port Select

A 74LS138 selects the input ports. Another 74LS138 selects the output ports.

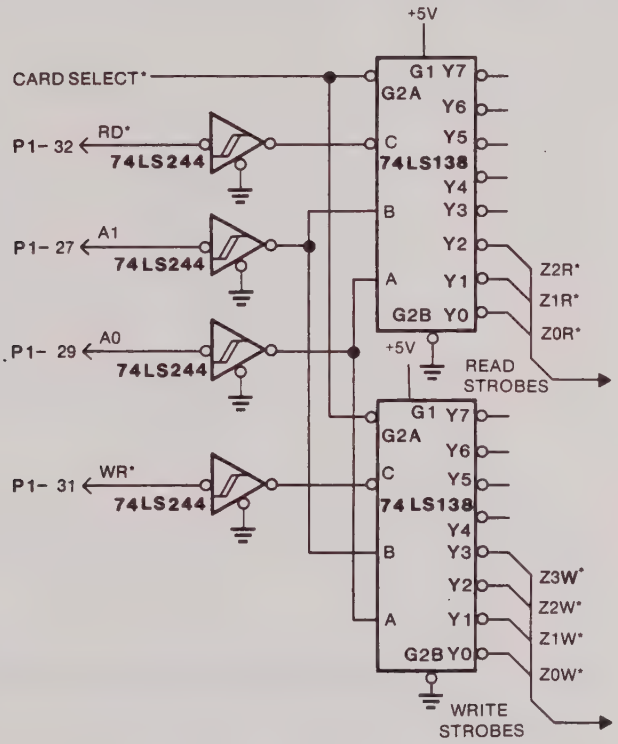


Figure 5-2. Port Select (7507)

Reset

A 74LS244 buffers the system reset signal which then resets all output ports.

Figure 5-3. Reset Buffer (7507)

Data Bus Buffer

The 74LS245, the data bus buffer, is enabled when the card is selected. It is normally pointing onto the card. It points the other way only if there is a card select and a read at the same time. This condition exists only when accessing an on-card input port.

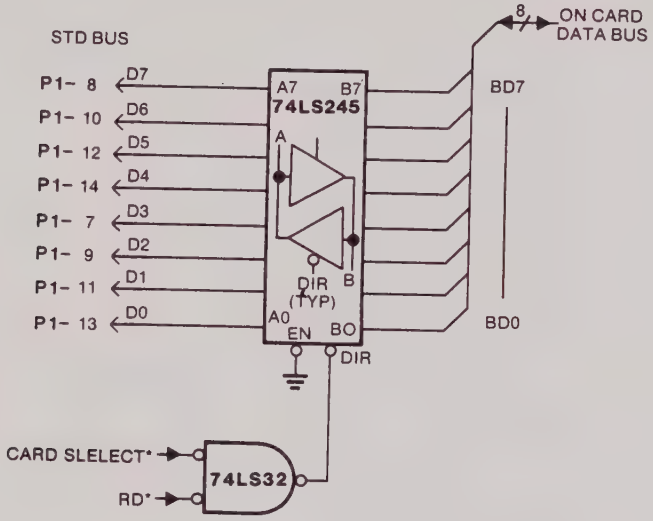


Figure 5-4. Data Bus Buffer (7507)

Input Ports

The 74LS240s are the input ports. These chips are all inverting buffers. The input data is always present at the input of the 74LS240 chips. When read select goes low on a port, the input data is gated through to the data bus.

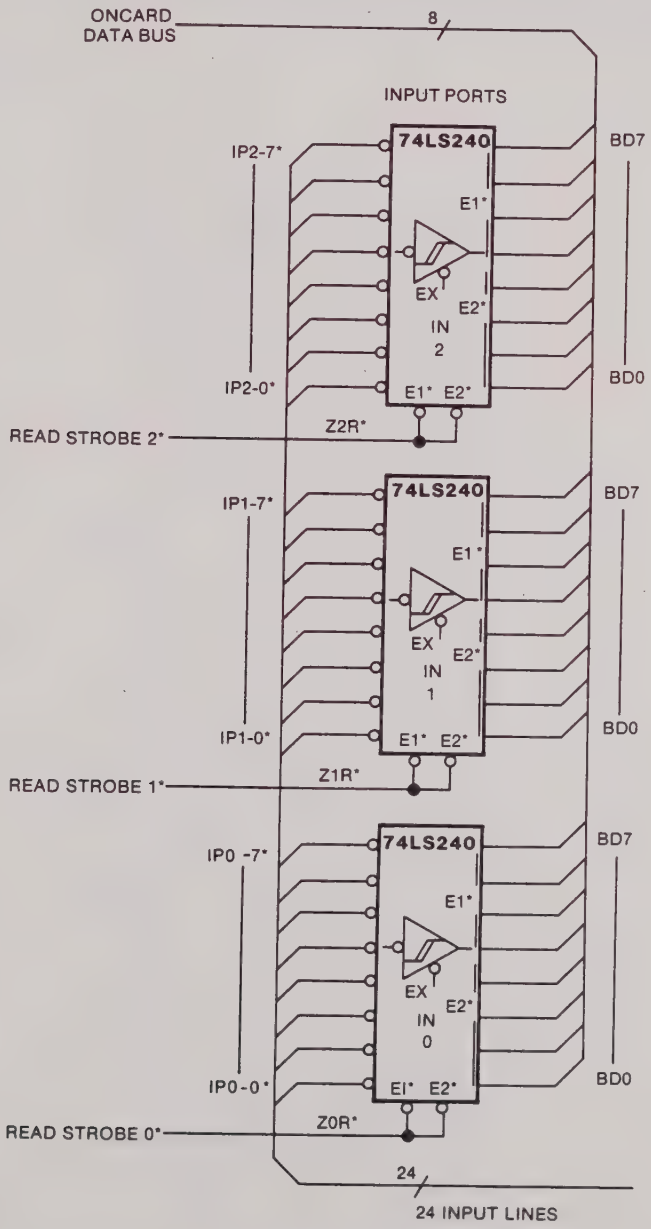


Figure 5-5. Input Ports (7507)

Output Ports

The 74LS273s are the data output ports. They are eight-bit latches. All of the latches are cleared by the reset line.

The inputs to the latches are connected to the data bus. Whenever the output strobe transitions from low to high, the data on the inputs is latched to the output lines.

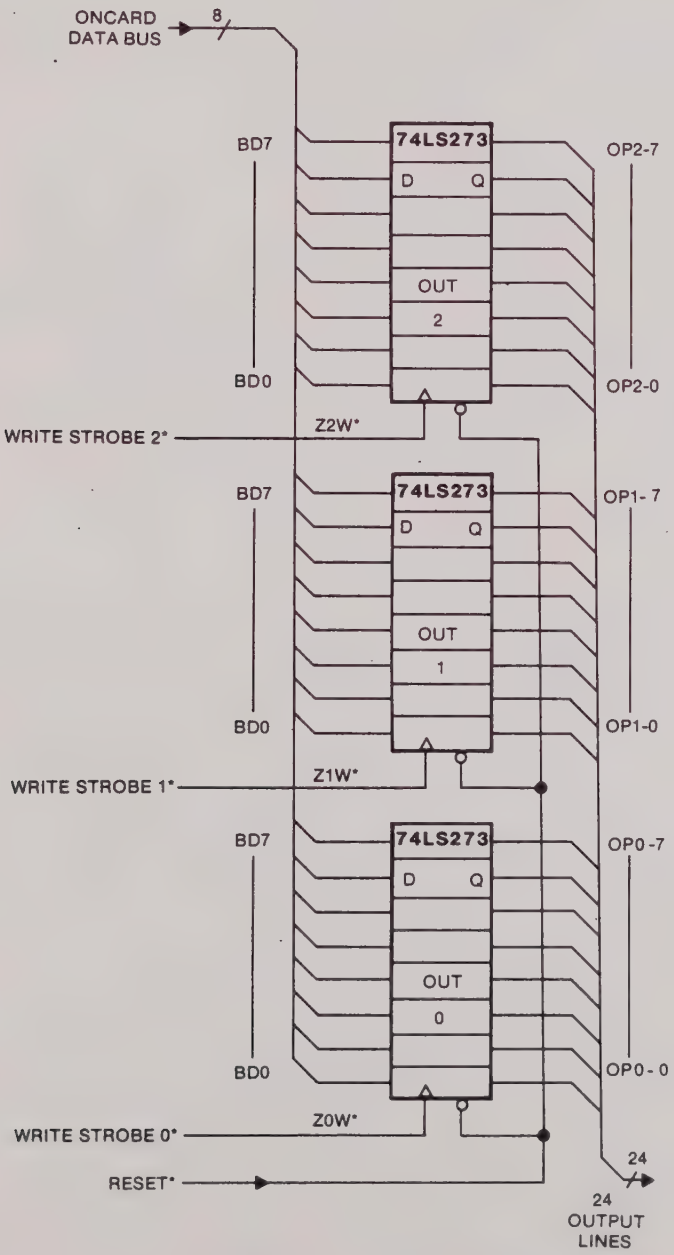


Figure 5-6. Output Ports (7507)

Power Port

A flip-flop is the output port for the power line. The output port is cleared (power-on condition) by the reset line. Each time the write-select line transitions from low to high, the state of D7 is latched into the flip-flop. If D7 is high (logic 1), the power is turned off. If D7 is low (logic 0), the power is turned on. When the output of the flip-flop is high, the output of the inverter is low, causing a base emitter current through the transistor. This current saturates the transistor junctions and power is applied to J1, pin 49. D1-4 is an LED that is illuminated by voltage on the power line.

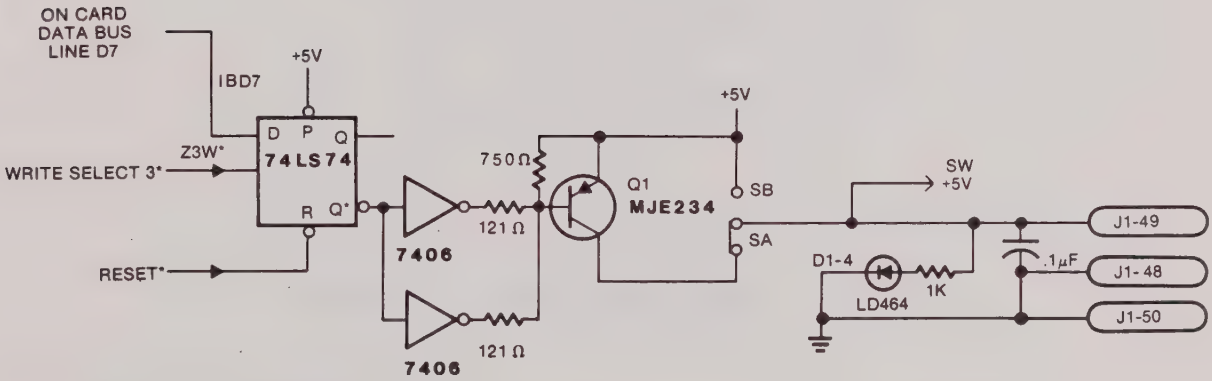


Figure 5-7. Power Port (7507)

Data Indicator LEDs

D1-1, D1-2, and D1-3 LEDs indicate the state of D7, D6, and D5, respectively, of output port 2.

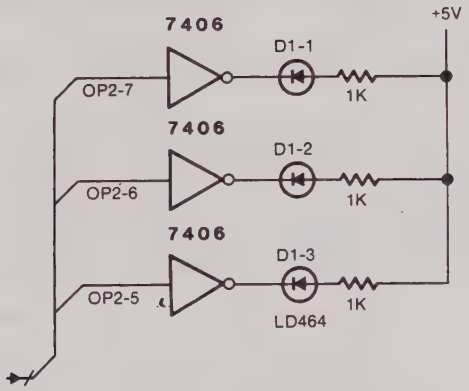


Figure 5-8. Indicator LEDs (7507)

Bidirectional Port Interface

All 24 bidirectional port lines have a circuit like the one shown in figure 5-9. For outputs, the 7406 is an "open-collector" driver that can only pull the line to ground. R2-6 is a pull-up resistor to pull the line back up. For inputs, the 7406 must be put into the off state which allows an external device to control the line. Also note that R1-4 and C8 form a "low-pass" filter to filter out noise on the input line.

It should be noted that Module 0* is connected to port 2, line 7, and this continues on to Module 23* which is connected to Port 0, line 0. The first line on the first port connects to the last module and the last line on the last port connects to the first module. The pull-up resistor is pulled up to SW +5V instead of +5V to prevent current flowing through the pull-up and into a rack module when power is not applied to the rack.

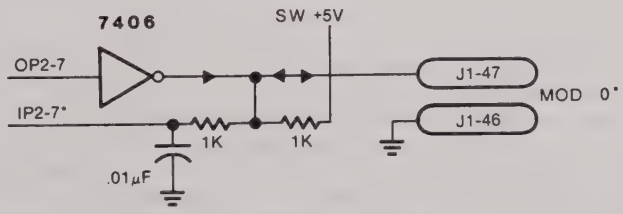


Figure 5-9. Bidirectional Port Interface (7507)

RETURN FOR REPAIR PROCEDURES

Domestic Customers:

1. Call CUSTOMER SERVICE at (408) 372-4593 (in California) or (800) 538-9570 (outside of California) 7 AM to 3 PM PST.

2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.

3. Please be sure to enclose a packing slip with the CRO number, the equipment serial number if applicable, and the reason for return. Also enclose the name and telephone number of the person we should contact (preferably the user).

4. Package the equipment in a solid cardboard box secured with packing material.

CAUTION: Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during handling. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, CA 93940
   Reference CRO #_____.

International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

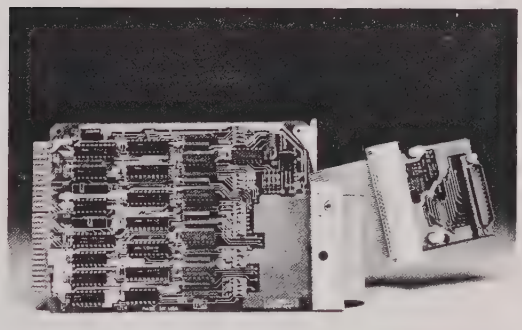
LIMITED WARRANTY:

Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. This liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair, or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller of the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

APPENDIX A
PIN 114 DATA SHEET

INTRODUCTION

The PIN 114 is hardware for a parallel interface based on the 7507. Software to run the interface is resident in Pro-Log's MP4/5 monitor program.



PIN114 PARALLEL INTERFACE FOR STD BUS

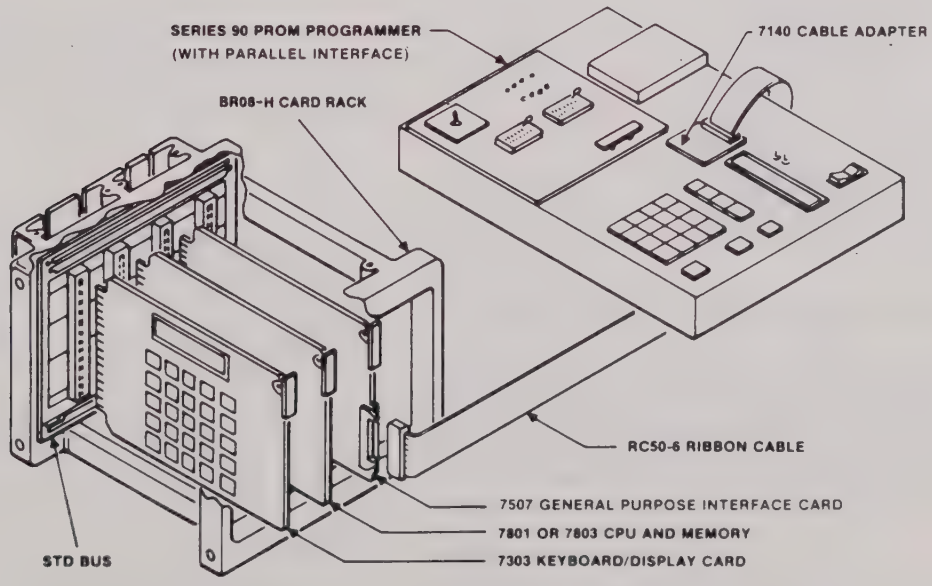
The PIN114 supplies an 8-bit parallel interface between STD BUS systems and Pro-Log's series 90 PROM programmers equipped with parallel interface options. The PIN114 provides the hardware interface that allows a bidirectional transfer of data fields between the user's STD BUS system and the PROM programmer. Data transfer is asynchronously controlled through handshake lines.

The PIN114 is immediately operational when interconnected to the STD BUS prototyping systems. Software to implement the interface is resident in the prototyping system monitor program and PROM programmer. When used with other STD BUS systems, specific software requirements and flowcharts may be found in the PROM programmer operating manuals.

FEATURES

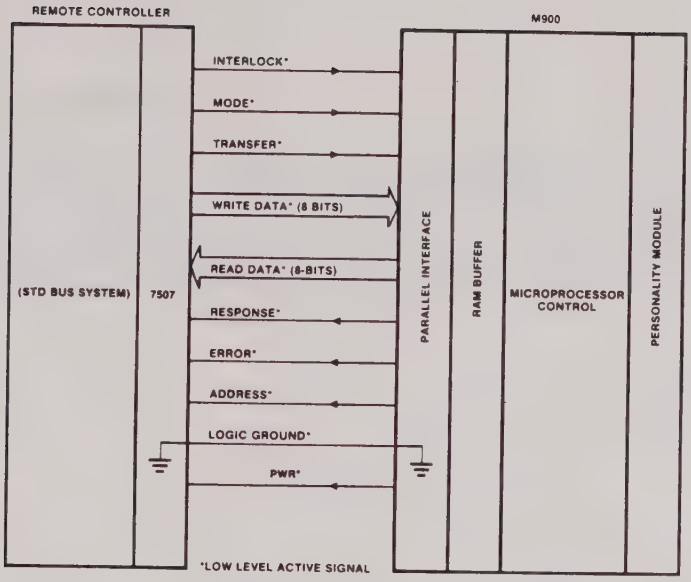
The PIN114 includes:

- **7507 general purpose interface card**
- **7140 parallel interface adapter**
- **RC50-6 ribbon cable interconnect**



System Interconnect

Figure A-1. PIN 114 Data Sheet



Parallel Interface — Data and Signals

The following diagrams describe the port/bit assignments on the 7507 when used as a PROM programmer.

PORT 50① — WRITE DATA							
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7 ◄——————————► Bit 0

PORT 51① — HANDSHAKE							
T	M	I	②	PWR	A	E	R
Out				In			

Bit 7 ◄——————————► Bit 0

PORT 52① — READ DATA							
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7 ◄——————————► Bit 0

① The 7507 is mapped to address 50-52 when shipped.
② Don't care.

BIT	SOURCE	LOGIC STATE ③
I	STD BUS System	1 = INTERLOCK* Active (low voltage) 0 = INTERLOCK* Inactive (high voltage)
M	STD BUS System	1 = MODE* Active (low voltage) 0 = MODE* Inactive (high voltage)
T	STD BUS System	1 = TRANSFER* Active (low voltage) 0 = TRANSFER* Inactive (high voltage)
PWR	Programmer	1 = Programmer power on 0 = Programmer power off
A	Programmer	1 = ADDRESS* Active (low voltage) 0 = ADDRESS* Inactive (high voltage) (ADDRESS* Inactive means data is present)
E	Programmer	1 = ERROR* Active (low voltage) 0 = ERROR* Inactive (high voltage)
R	Programmer	1 = RESPONSE* Active (low voltage) 0 = RESPONSE* Inactive (high voltage)

*Low Level Active

③ Handshake lines are active low electrically, active high on the STD Data Bus or the processor's accumulator.

NOTE: When not used for the PROM programmer interface, the 7507 and RC50-6 can be used as an industrial I/O interface to OPTO-22, or equivalent module mounting racks, or as a general purpose TTL I/O card with 24 bit-programmable bidirectional lines.

USER'S MANUAL

To obtain the user's manual for the PIN114, ask for Pro-Log document #106667.

Figure A-2. PIN 114 Data Sheet (continued)

Appendix B

DOCUMENTATION

REFERENCE DRAWINGS

The schematic (figure B-1) and assembly drawing (figure B-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. These drawings may differ in some respects from the card you receive from Pro-Log. If you require the specific revision documents of the schematic and assembly for the board shipped, please use the information request form in the back of this manual to order them.

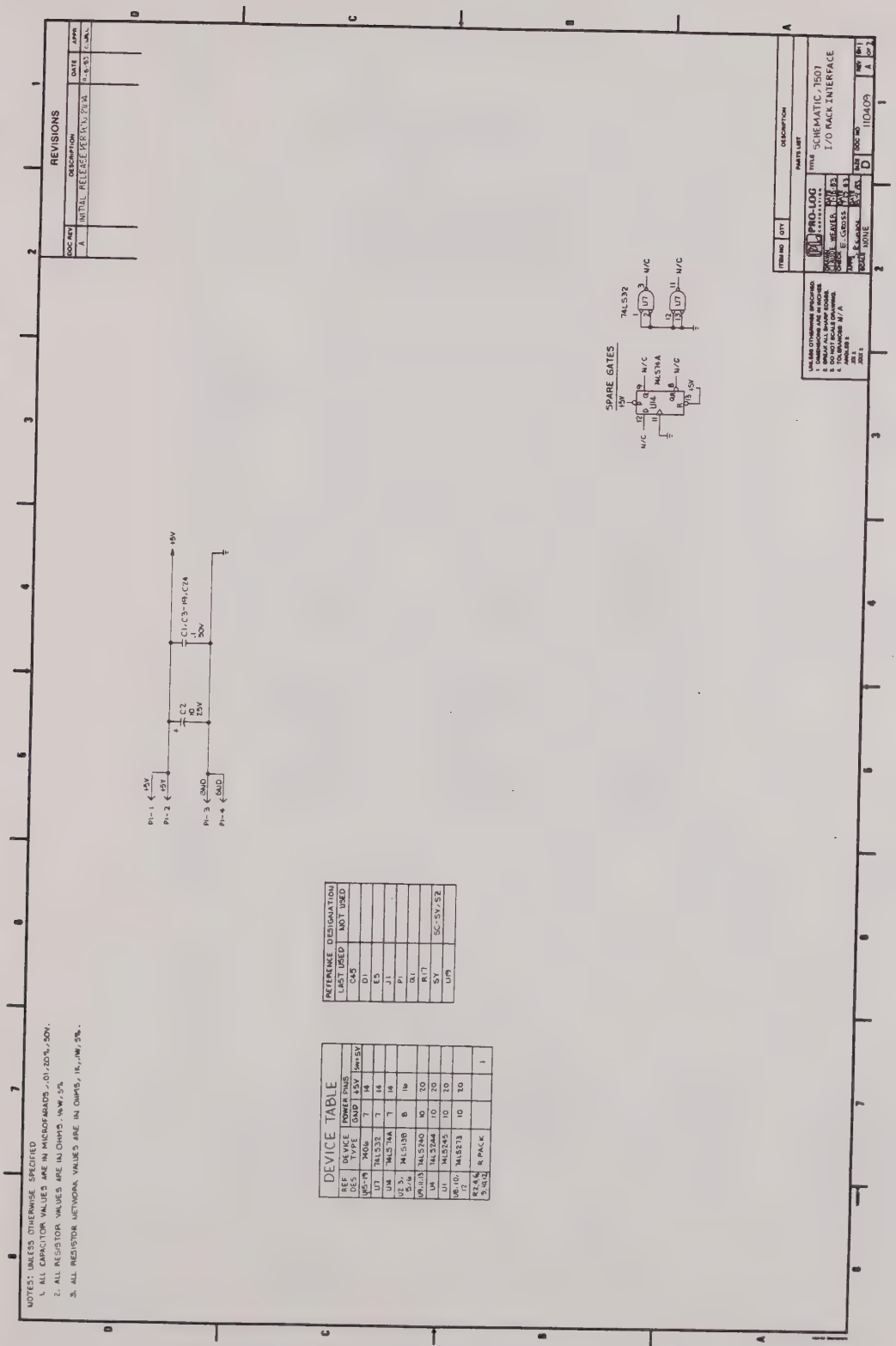


Figure B-1. Schematic (7507), Sheet 1 of 2

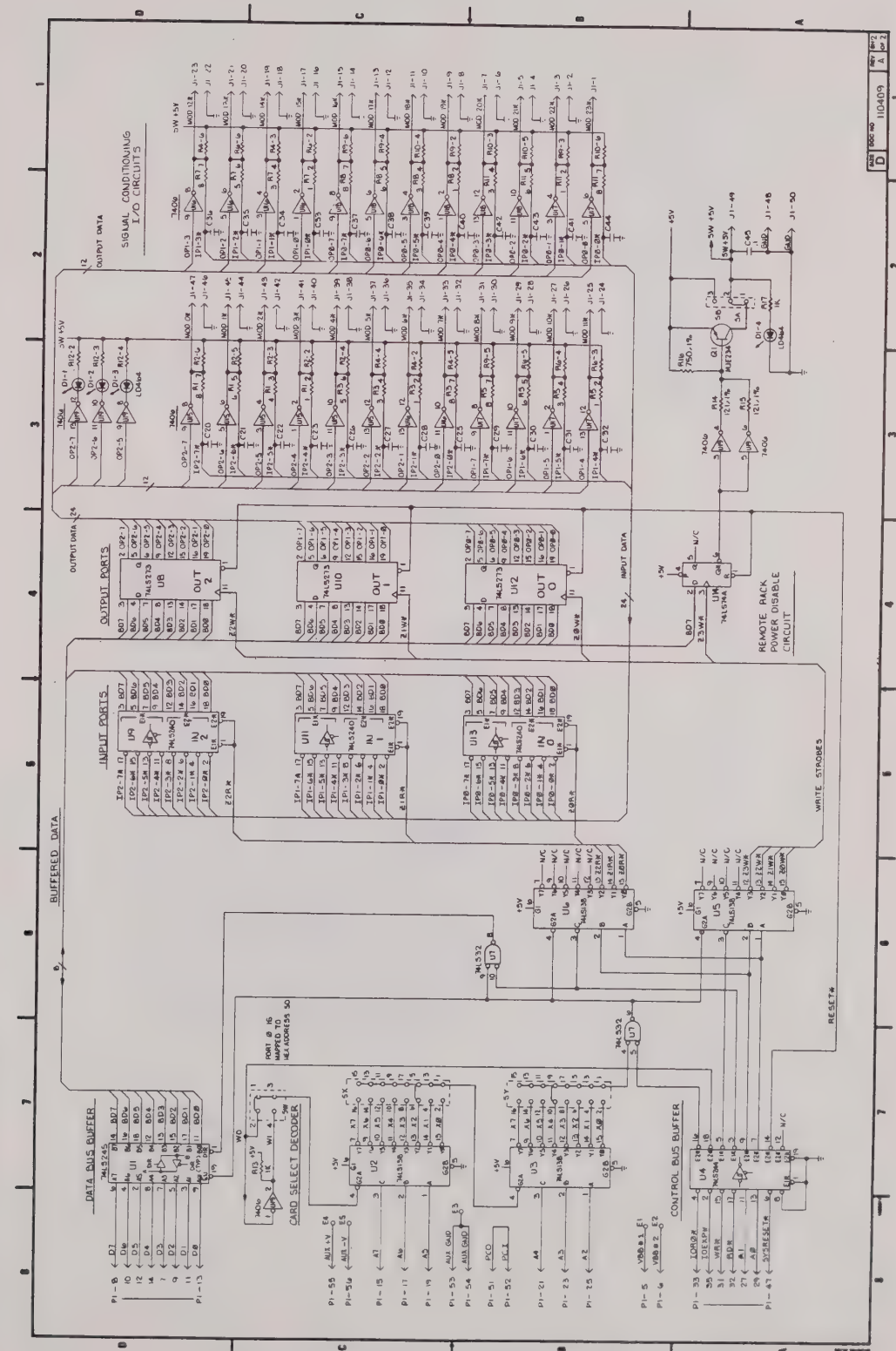


Figure B–2. Schematic (7507), Sheet 2 of 2

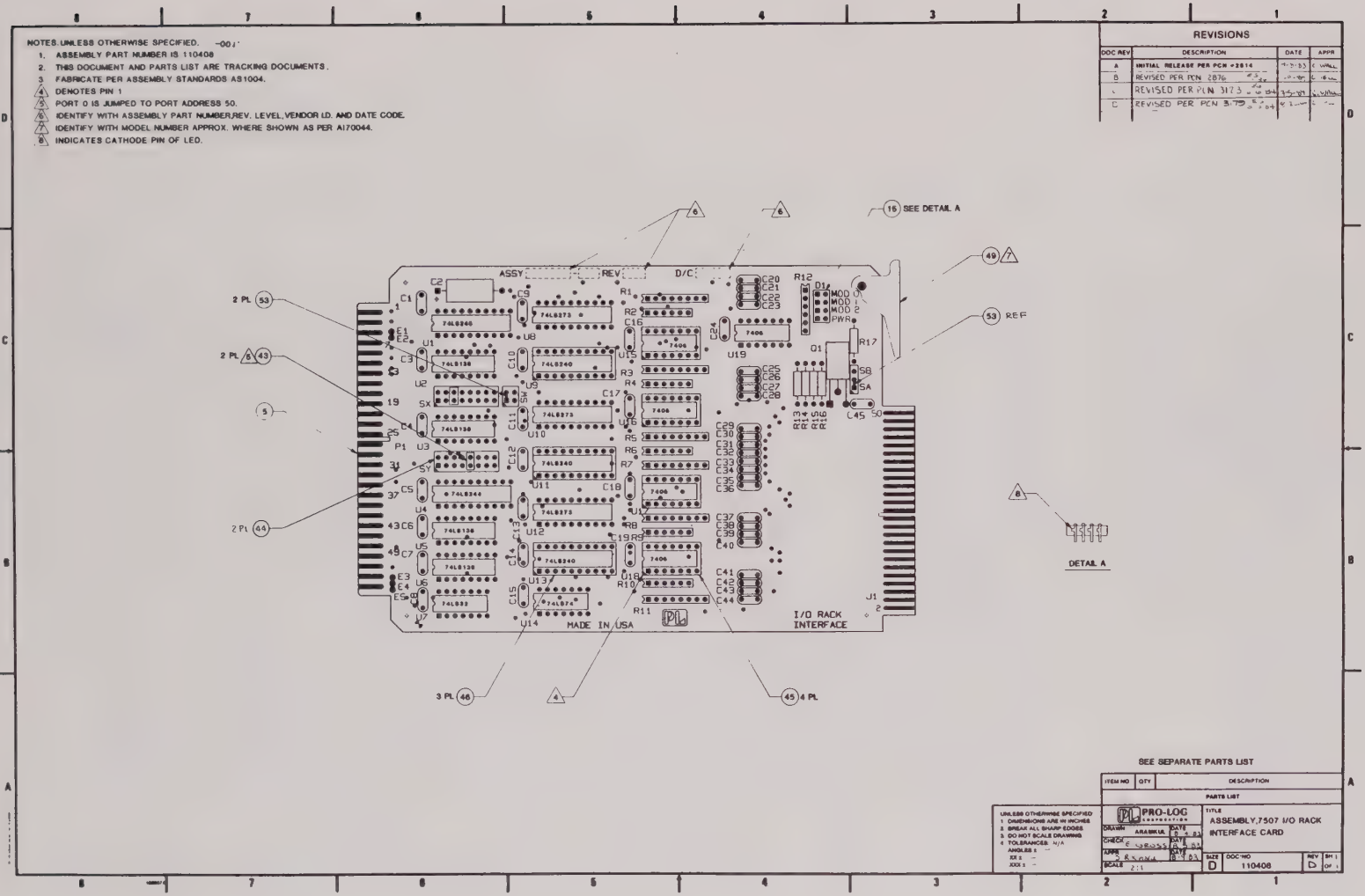


Figure B-3. Assembly (7507)

Cut Here

LD

FOLD

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- ☐ Designer Software
- ☐ Design Courses and Seminars
- ☐ Other _____

- ☐ I am currently using Pro-Log equipment.
- ☐ Add my name to your mailing list.
- ☐ Please have a Sales Representative contact me.

Reader Comments: _____

Name _____ City _____

Company _____ State _____ Zip _____

Address _____ Telephone _____

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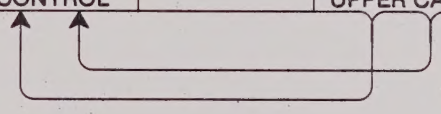
HEX				MSD	p=1	8	9	A	B	C	D	E	F
					p=0	0	1	2	3	4	5	6	7
	BITS				b8	p	p	p	p	p	p	p	p
					b7	0	0	0	0	1	1	1	1
					b6	0	0	1	1	0	0	1	1
LSD	b4	b3	b2	b5 / b1	0	1	0	1	0	1	0	1
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
1	0	0	0	1	SOH	DC1	!	1	A	Q	a	q
2	0	0	1	0	STX	DC2	"	2	B	R	b	r
3	0	0	1	1	ETX	DC3	#	3	C	S	c	s
4	0	1	0	0	EOT	DC4	$	4	D	T	d	t
5	0	1	0	1	ENQ	NAK	%	5	E	U	e	u
6	0	1	1	0	ACK	SYN	&	6	F	V	f	v
7	0	1	1	1	BEL	ETB	'	7	G	W	g	w
8	1	0	0	0	BS	CAN	(	8	H	X	h	x
9	1	0	0	1	HT	EM	)	9	I	Y	i	y
A	1	0	1	0	LF	SUB	*	:	J	Z	j	z
B	1	0	1	1	VT	ESC	+	;	K	[	k	{
C	1	1	0	0	FF	FS	,	<	L	\	l	|
D	1	1	0	1	CR	GS	—	=	M	]	m	}
E	1	1	1	0	SO	RS	.	>	N	^	n	~
F	1	1	1	1	SI	US	/	?	O	_	o	DEL
					CONTROL				UPPER CASE		LOWER CASE	

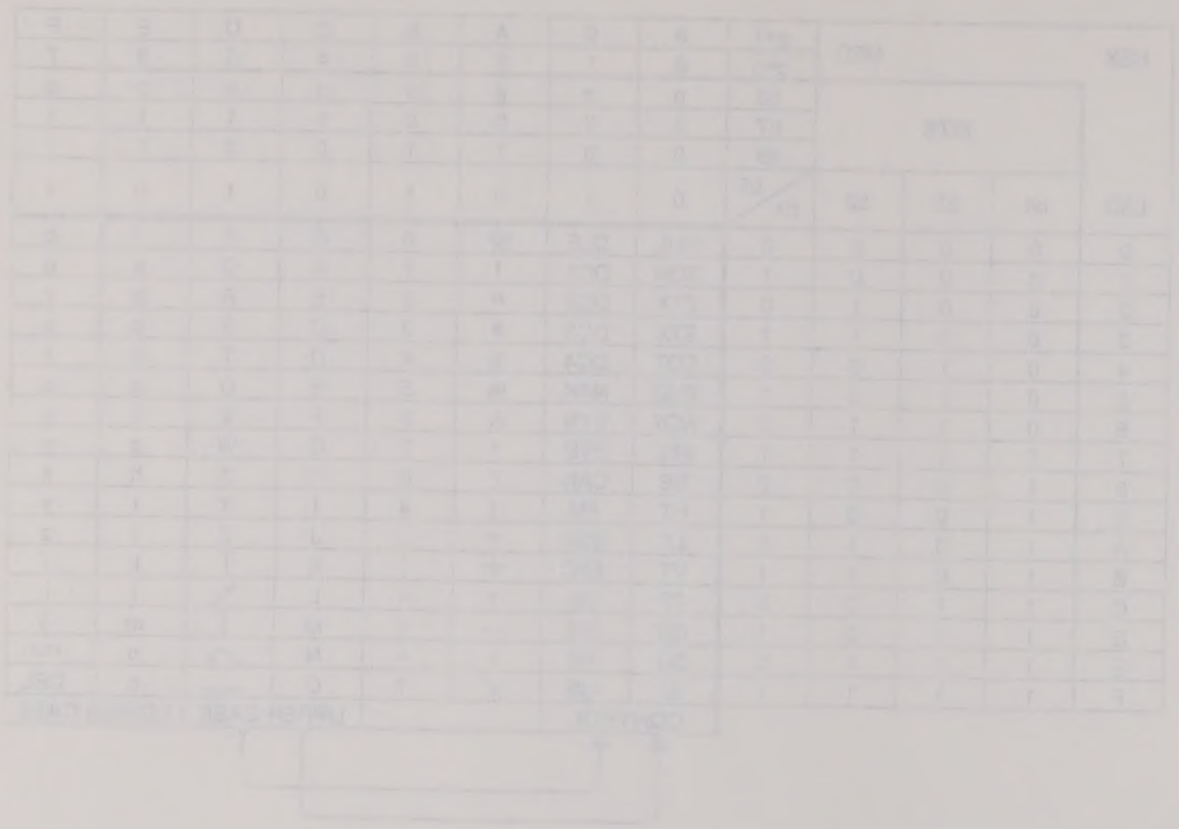


CONTROL CHARACTERS AND STANDARD KEYBOARD CONTROL SHIFT CHARACTERS

CTRL	@	NUL	Null	CTRL	K	VT	Vertical Tabulation	CTRL	V	SYN	Synchronous Idle
CTRL	A	SOH	Start of Heading	CTRL	L	FF	Form Feed	CTRL	W	ETB	End of Transmission Block
CTRL	B	STX	Start of Text	CTRL	M	CR	Carriage Return	CTRL	X	CAN	Cancel
CTRL	C	ETX	End of Text	CTRL	N	SO	Shift Out	CTRL	Y	EM	End of Medium
CTRL	D	EOT	End of Transmission	CTRL	O	SI	Shift In	CTRL	Z	SUB	Substitute
CTRL	E	ENQ	Enquiry	CTRL	P	DLE	Data Link Escape	CTRL	[	ESC	Escape
CTRL	F	ACK	Acknowledge	CTRL	Q	DC1	Device Control 1	CTRL	\	FS	File Separator
CTRL	G	BEL	Bell	CTRL	R	DC2	Device Control 2	CTRL	]	GS	Group Separator
CTRL	H	BS	Backspace	CTRL	S	DC3	Device Control 3	CTRL	^	RS	Record Separator
CTRL	I	HT	Horizontal Tabulation	CTRL	T	DC4	Device Control 4	CTRL	_	US	Unit Separator
CTRL	J	LF	Line Feed	CTRL	U	NAK	Negative Acknowledge			DEL	Delete

NOTE: The table above lists the keyboard character to be pressed with the Control key, the mnemonic for the function to be performed, and the description of the function. While the keyboard character is listed as uppercase, either uppercase or lowercase characters may be used.

ASCII Code Assignments



USER'S MANUAL

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Telex: 171879, TWX: 910-360-7082

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